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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

APUS_KL
ACER KBL R + MX130
A01 BUILD

2018.08.07

21-OCT-2002		
DATE	CHANGE NO.	REV

				<div>INVENTEC</div>			
				TITLE			
DESIGN / DRAWER				MODEL,PROJECT,FUNCTION			
XXX							
BRYAN CHIOU							
TICKY TSAI							
FILE NAME							
R10_TOPAZ_WS							
PCB PIN							
60xxxxxxxxxx							

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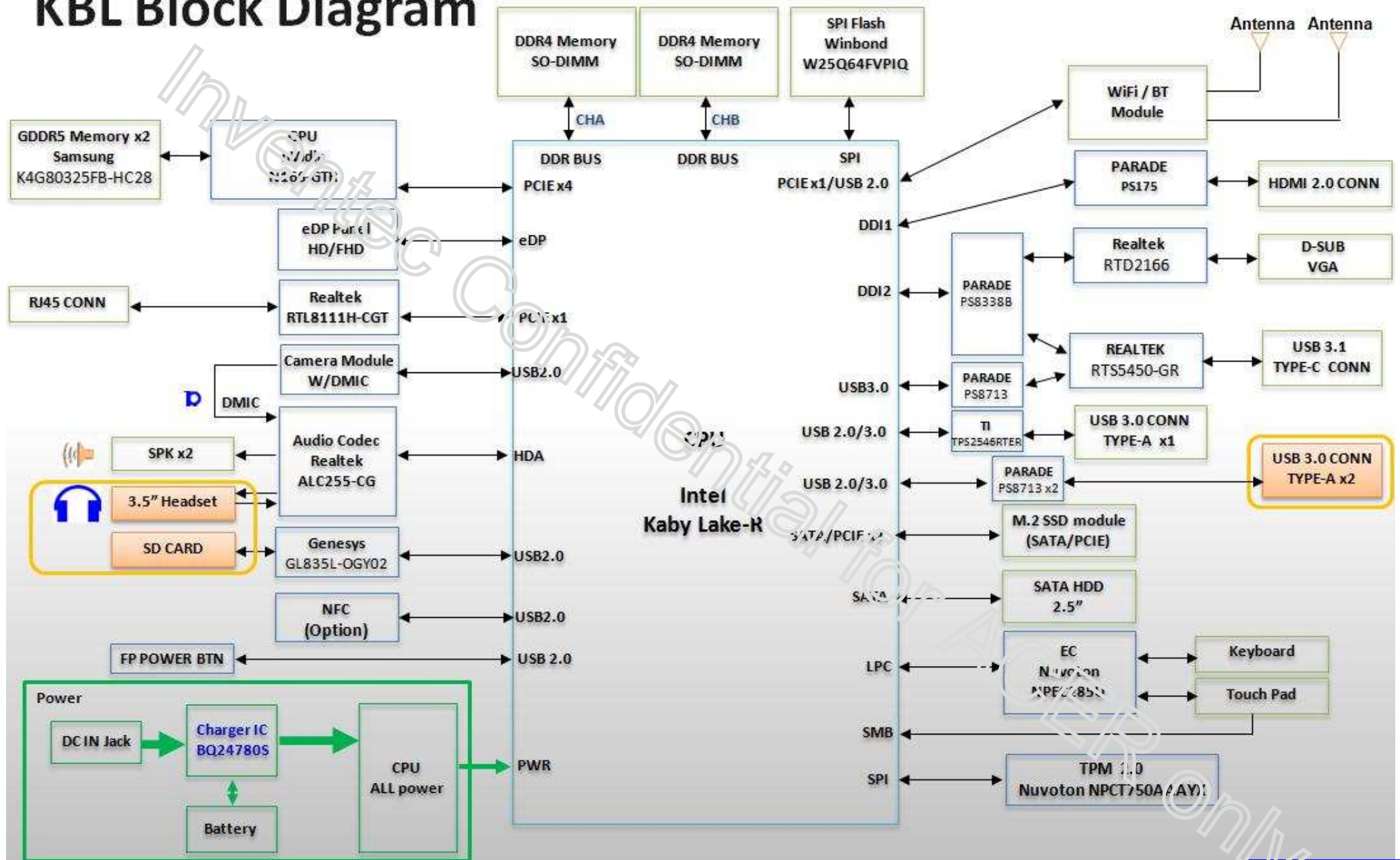
51 USB3.0 PORT 3
52 TYPEC ADP IN
53 TYPEC USB REDRIVER
54 USB TYPE C CONTROLLER
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56 EDP CONN
57 DP MUX
58 DP2HDMI CONVERTER
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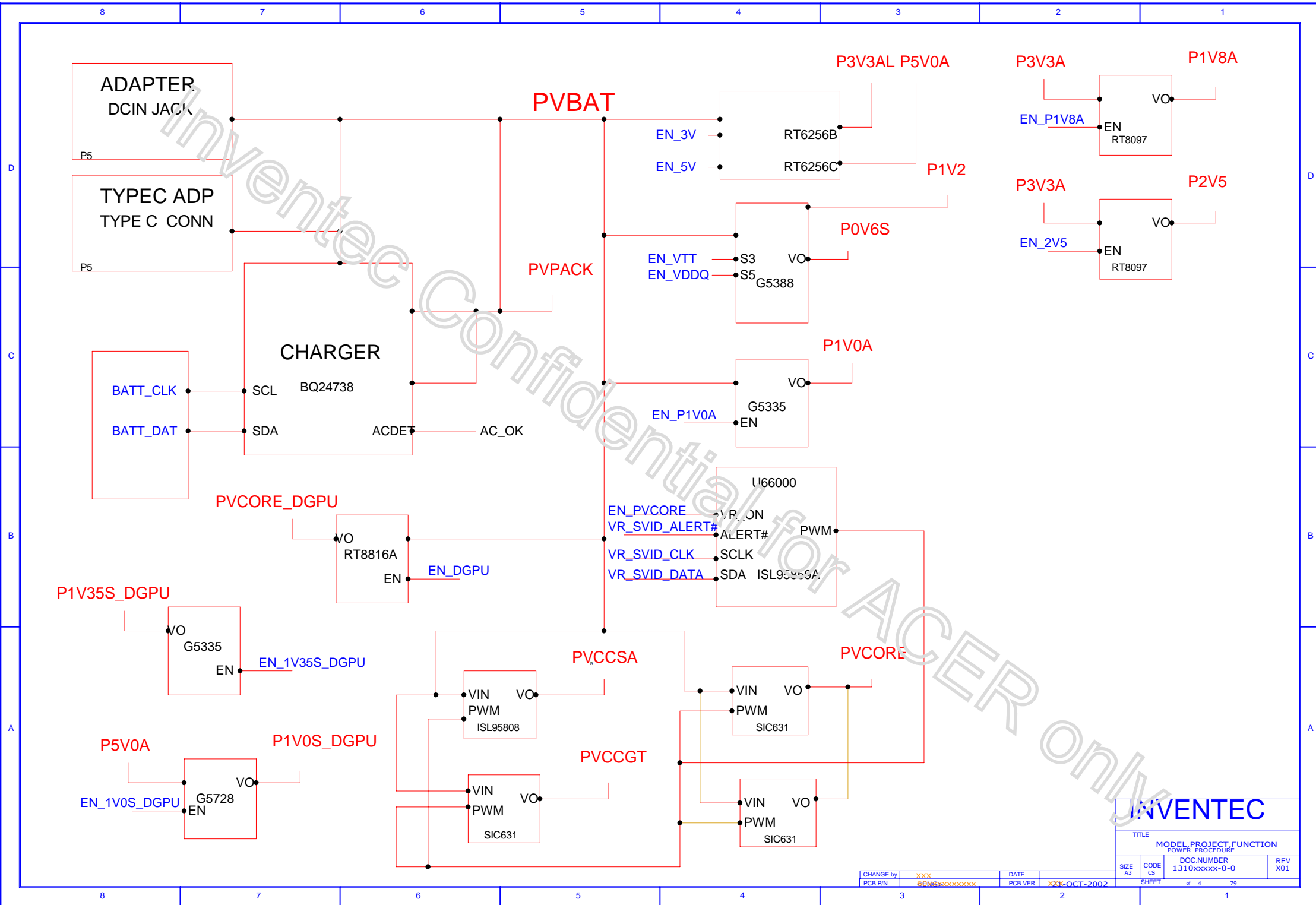
KBL Block Diagram



INVENTEC

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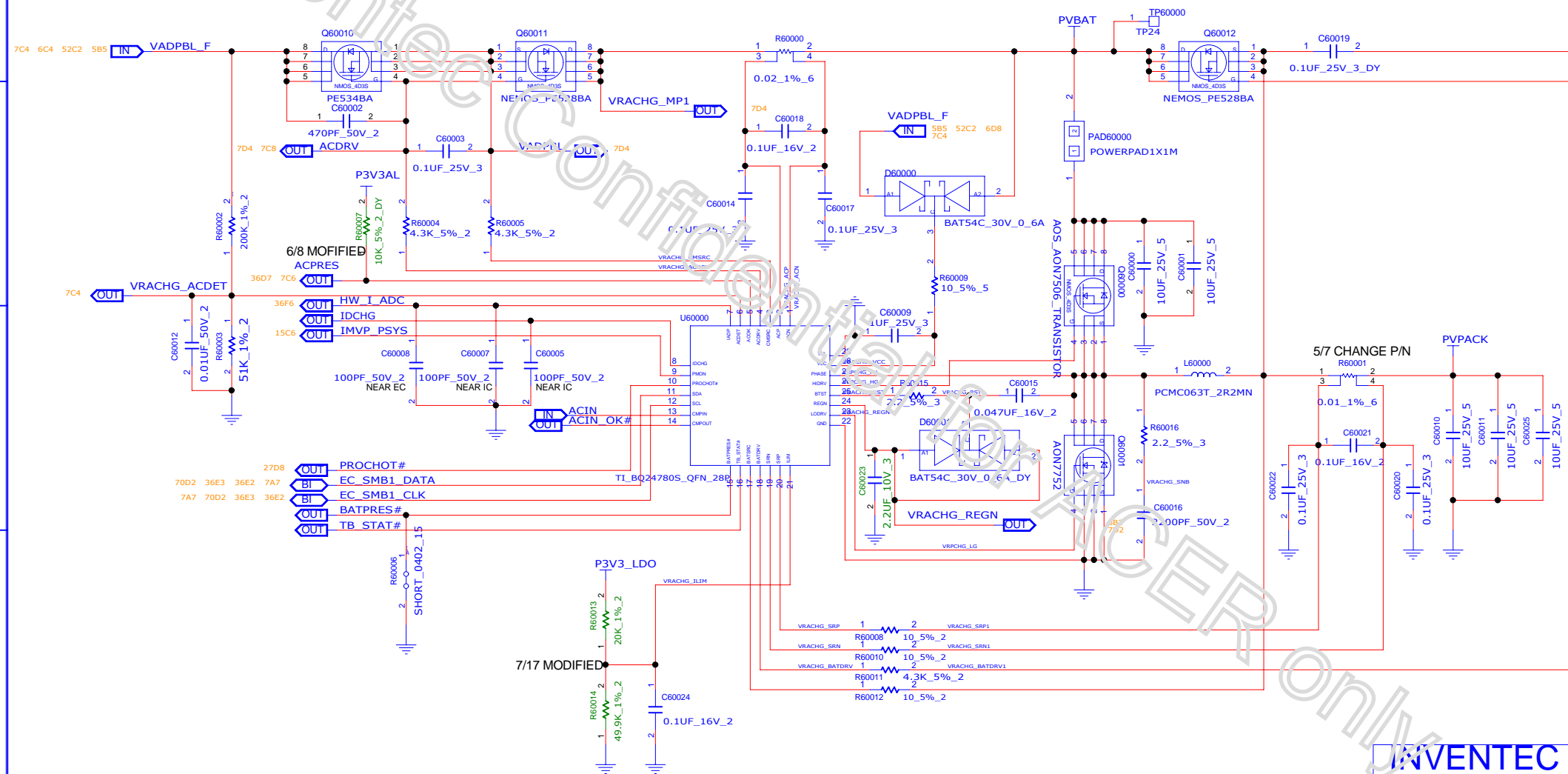


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INVENTEC

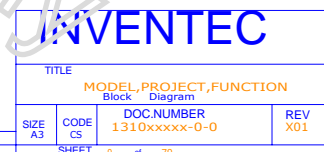
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Block Diagram			
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C								
B								
A								
	8	7	6	5	4	3	2	1

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INVENTEC			
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CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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D

C

B

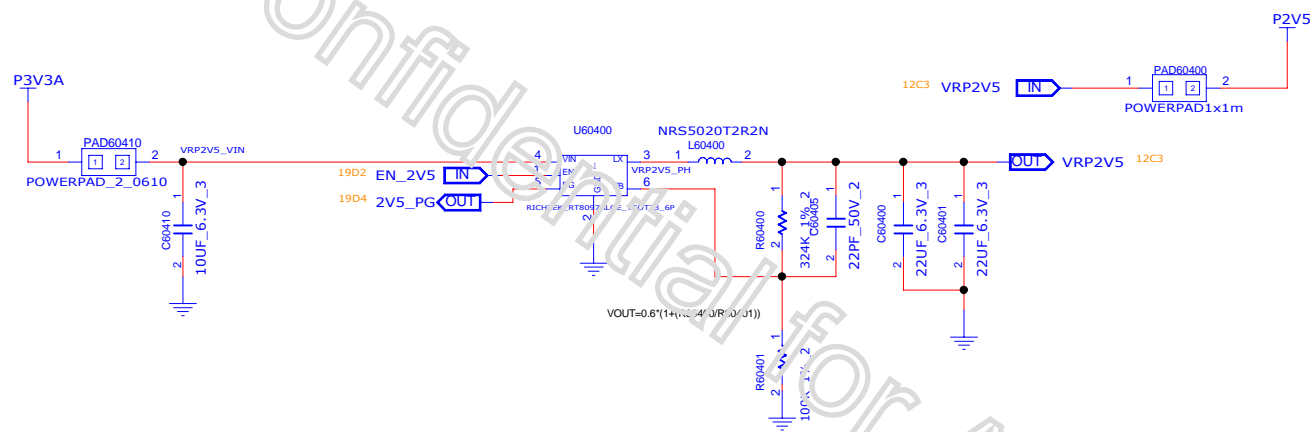
A

D

C

B

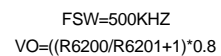
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**INVENTEC**TITLE
MODEL, PROJECT, FUNCTION
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SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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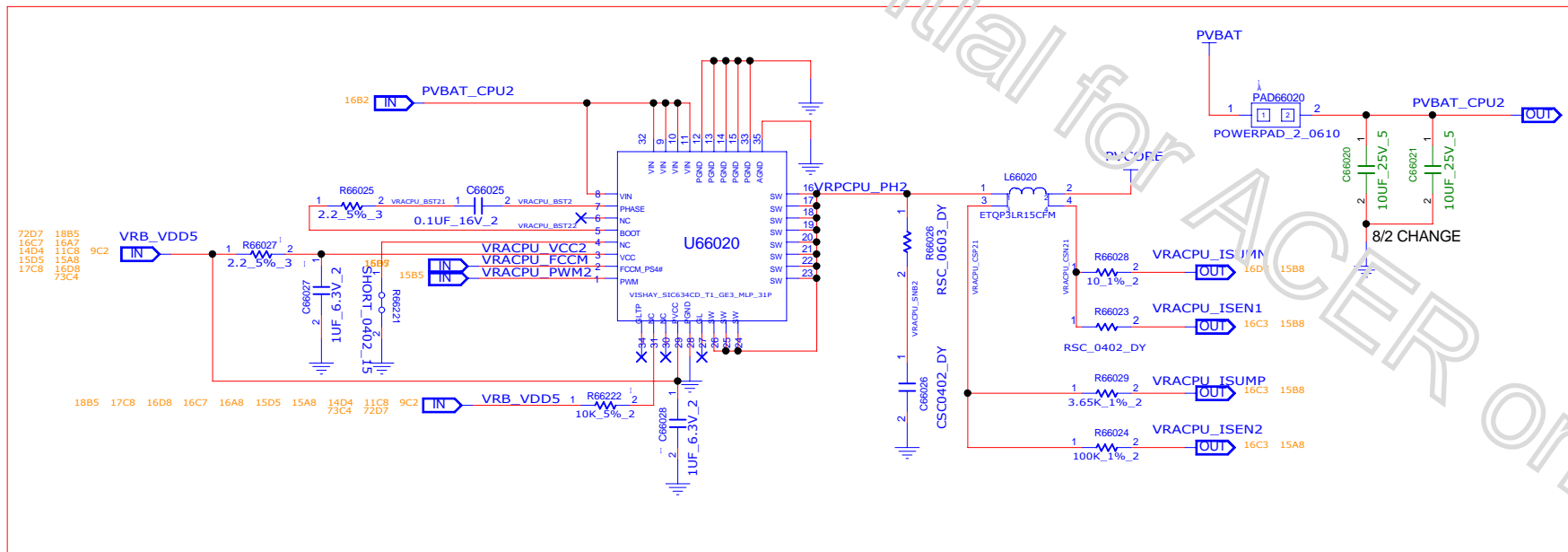
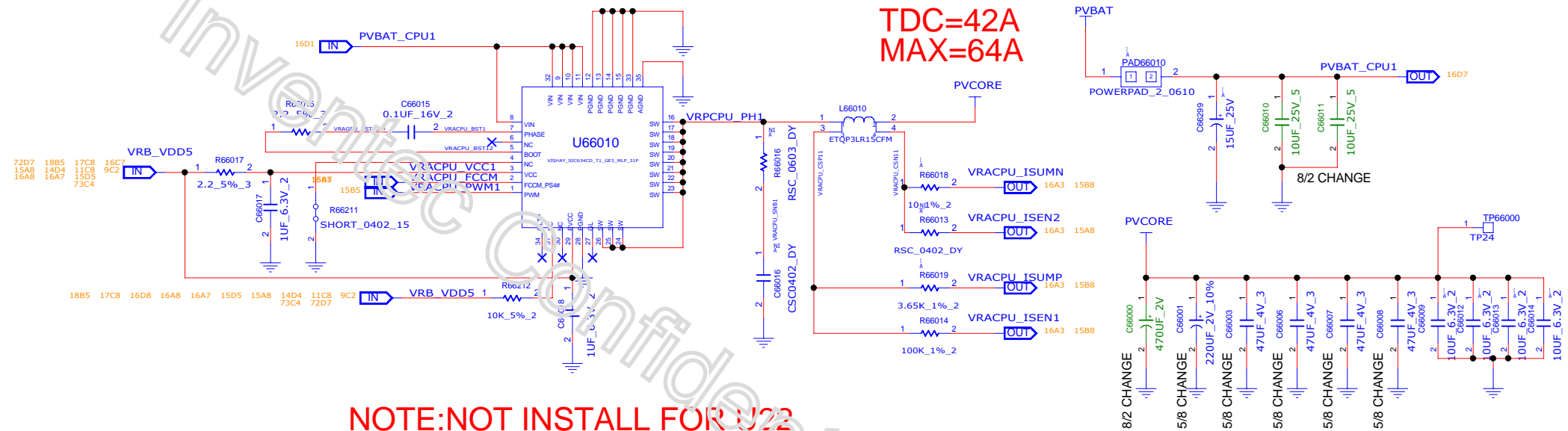
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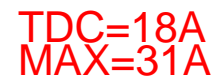




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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

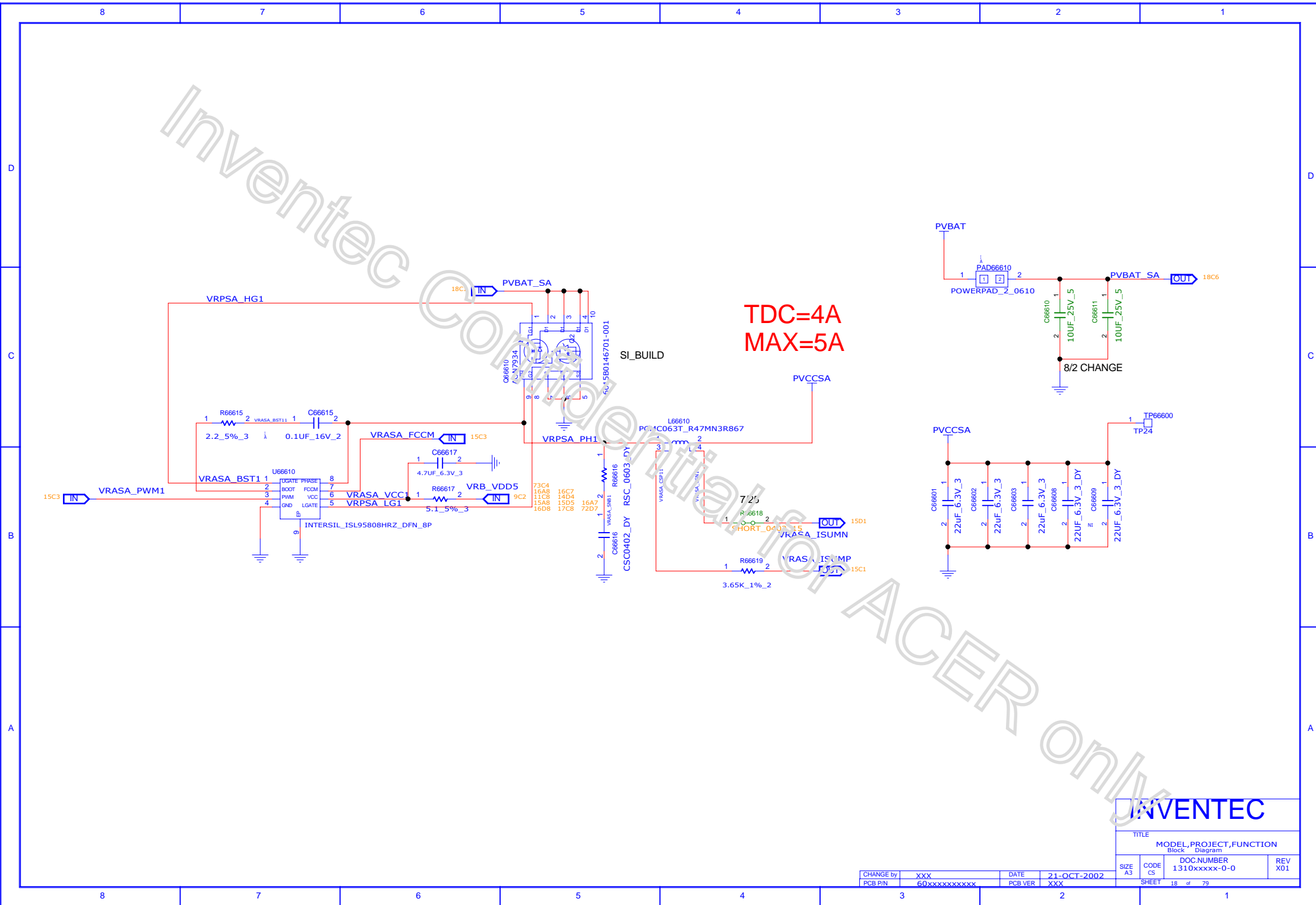


NOTE:ONE PHASE FOR U22



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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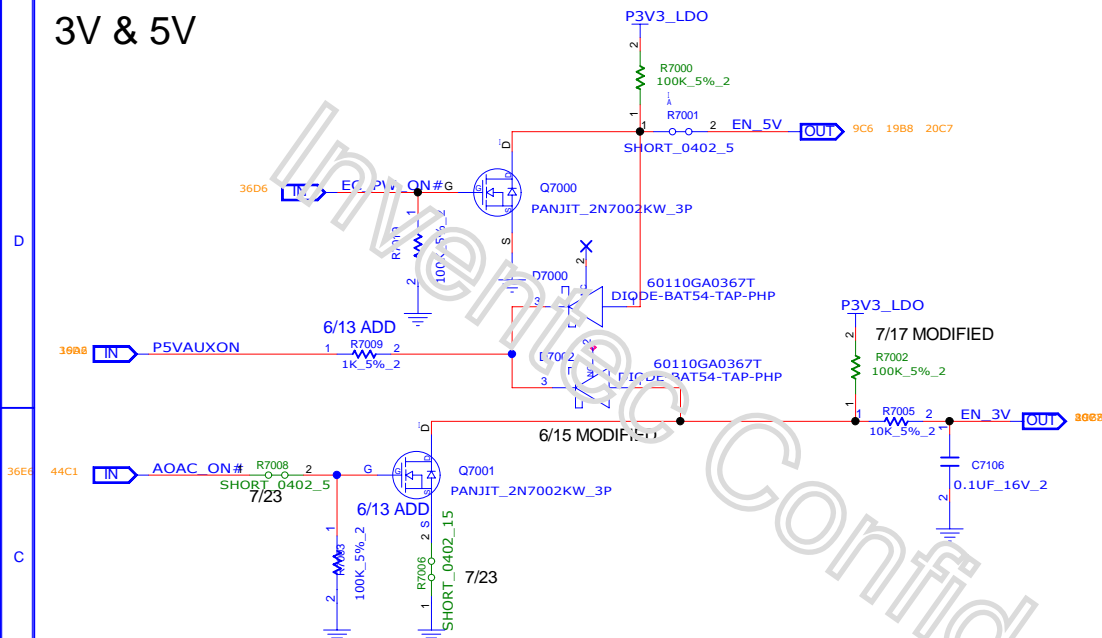


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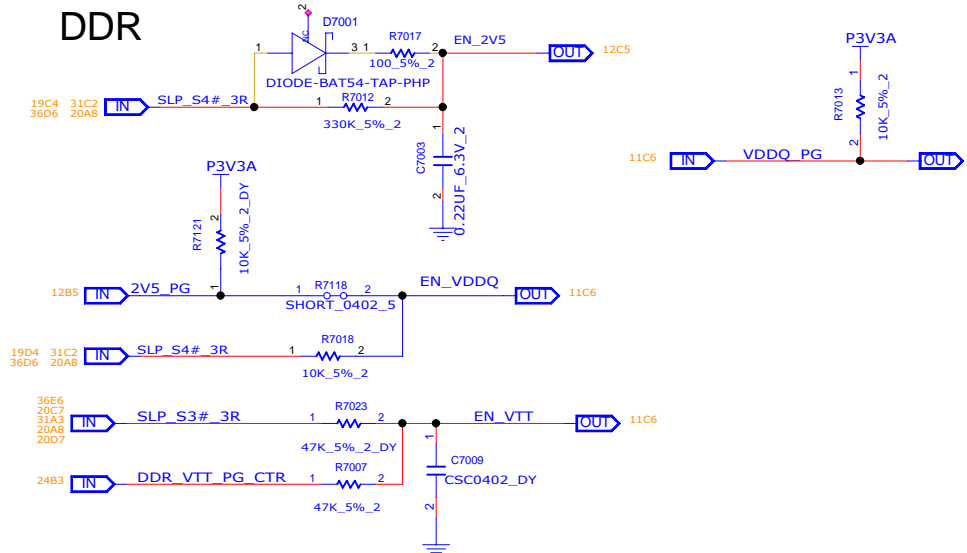
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Block Diagram			
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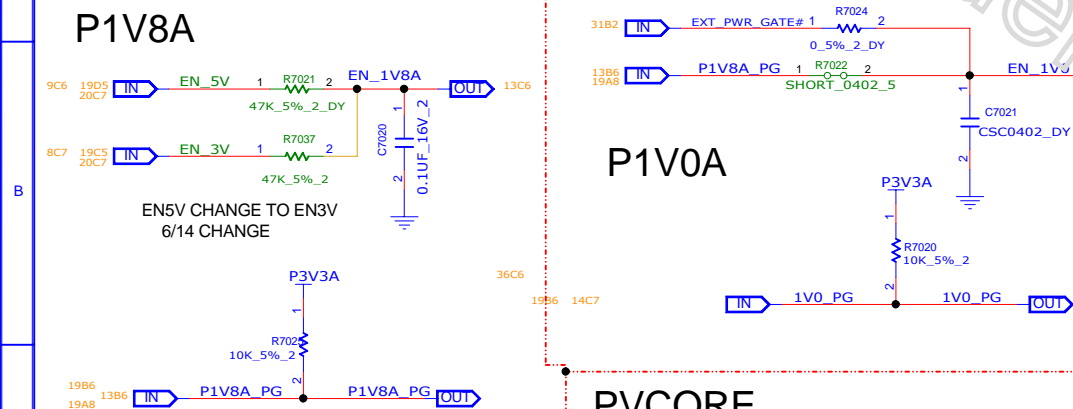
3V & 5V



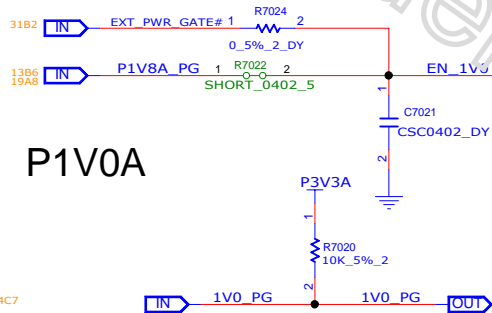
DDR



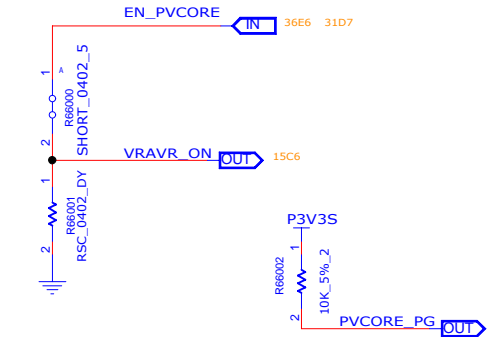
P1V8A



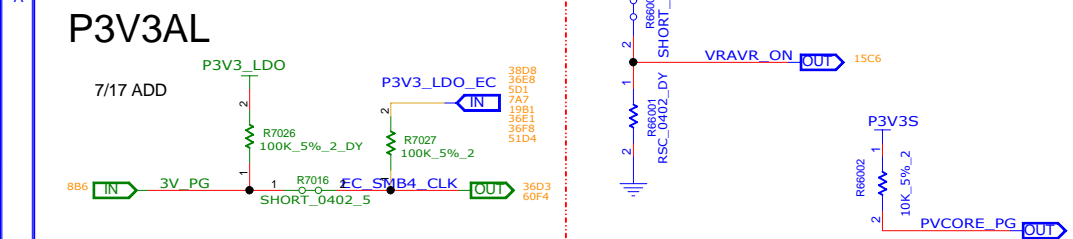
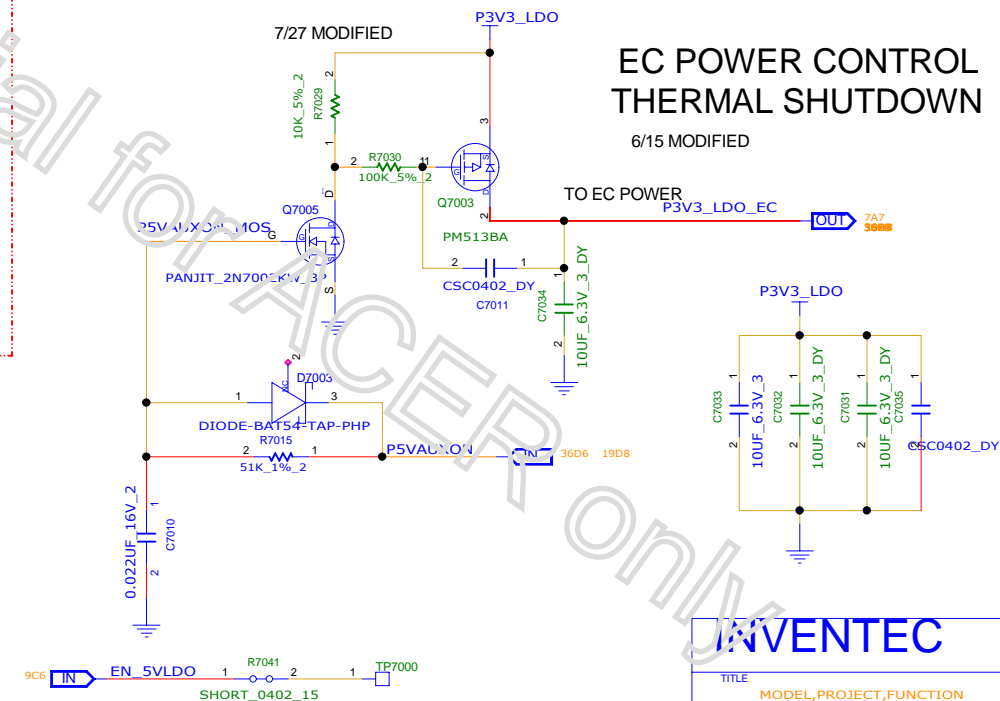
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PVCORE



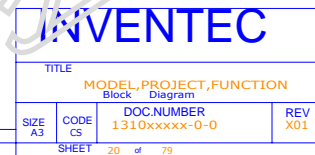
P3V3AL

EC POWER CONTROL
THERMAL SHUTDOWN

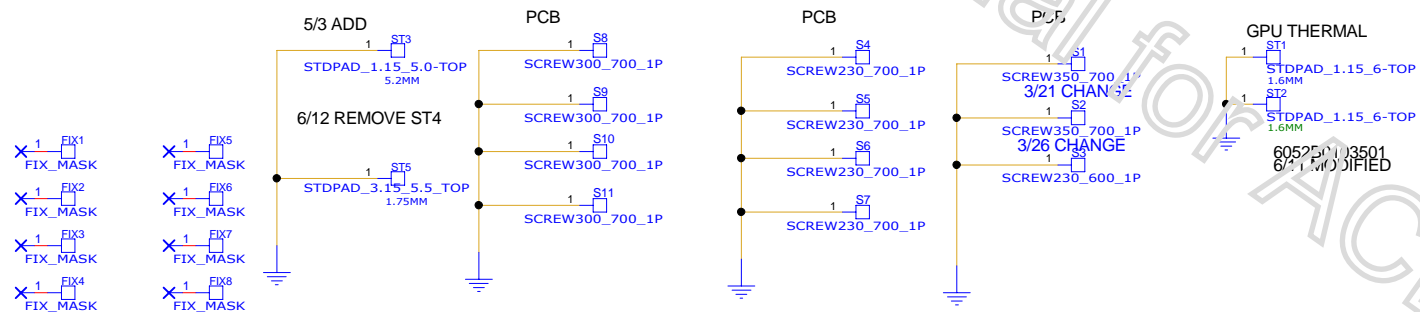
INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

TITLE	MODEL, PROJECT, FUNCTION
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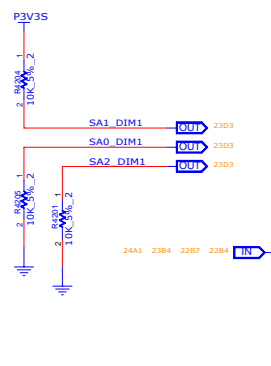
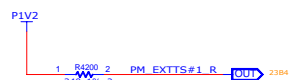
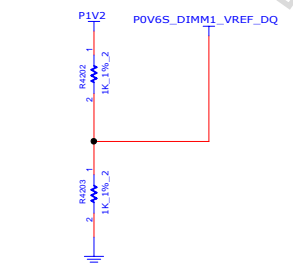
REFERENCE 0-49(PCB SCREW)



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Block Diagram			
SIZE	CODE	DOC NUMBER	REV
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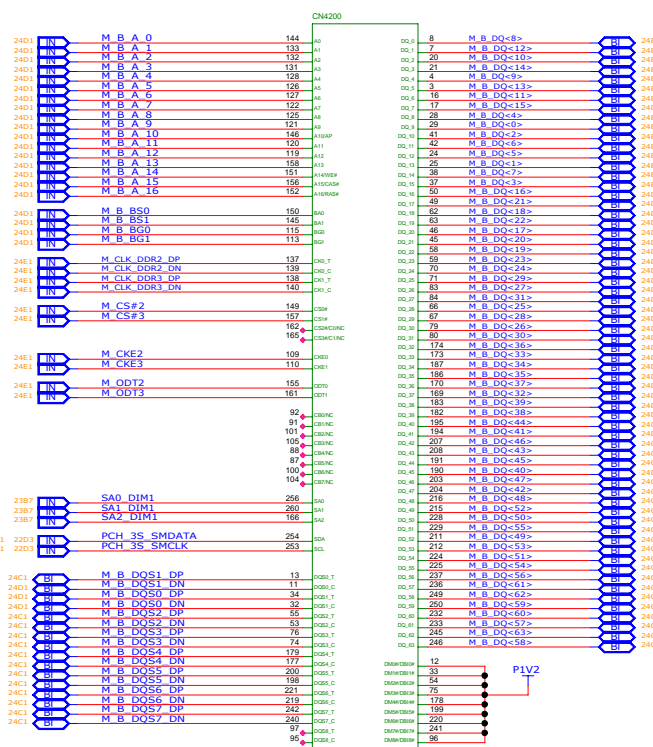
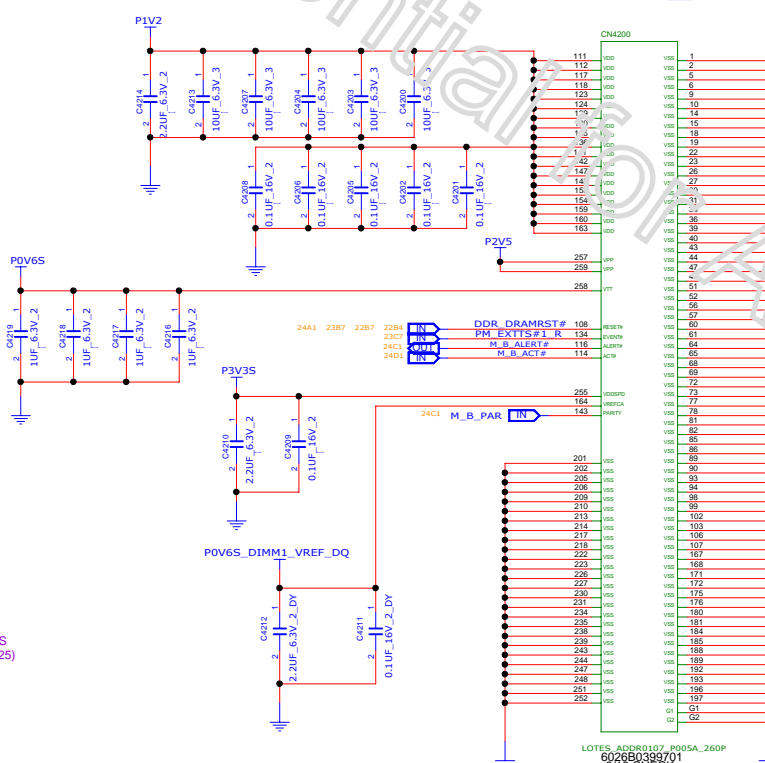
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

CHB SODIMM 1 H=4.15MM



NOTE:
SO-DIMM SPD ADDRESS IS 0X44
SO-DIMM TS ADDRESS IS 0X34

PLACE C4120 WITHIN 200 MILS
FROM THE SODIMM - 1 (CN4125)

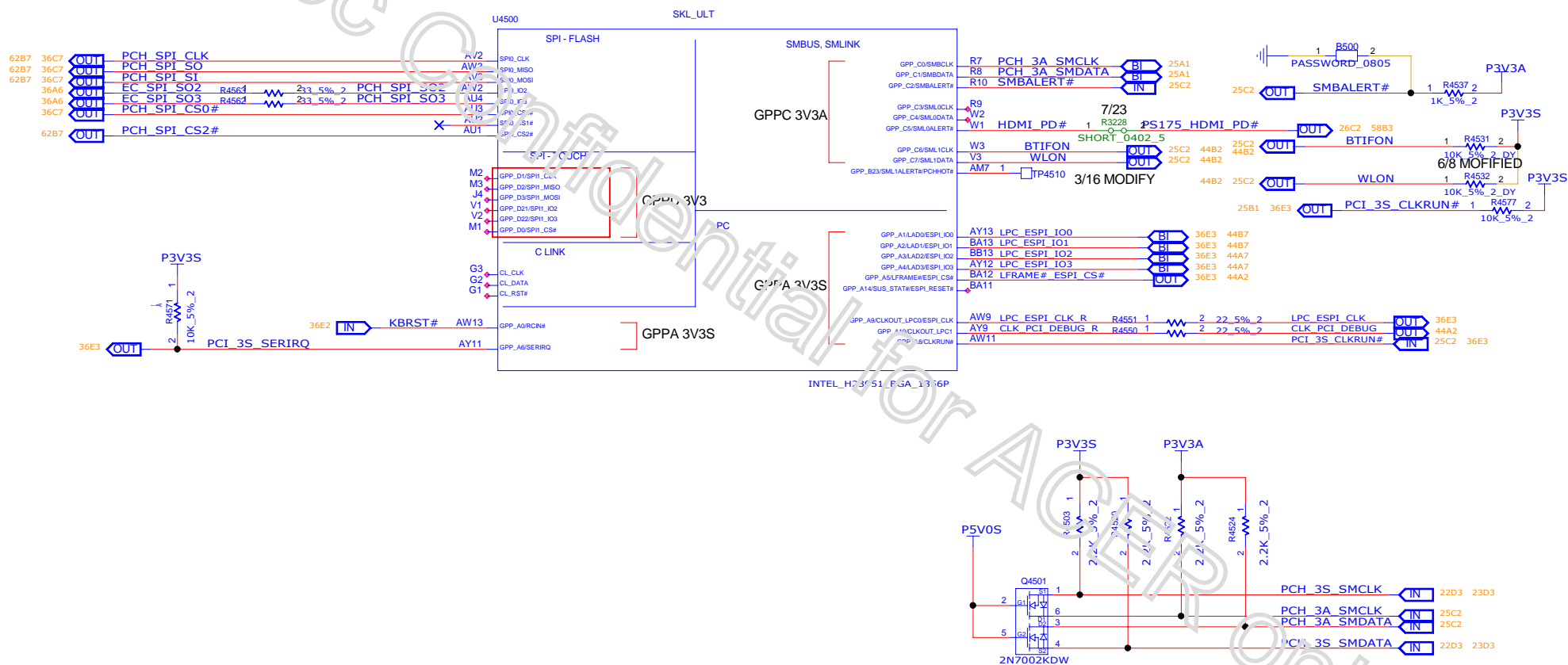


LOTES_ADDR0107_P005A_26
 7/20 CHANGE
 6026B0346601-002

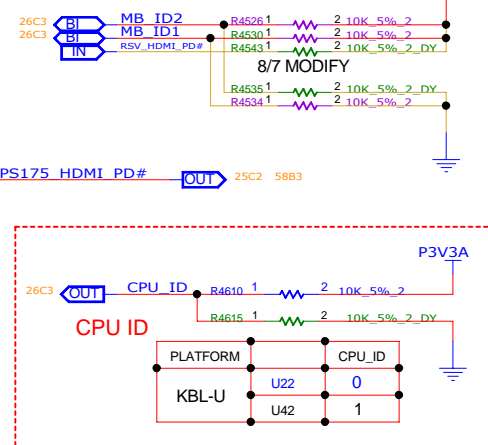
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CHANGE BY	XXX	DATE	21-OCT-2002	A3	CS	1310xxxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 23 of 79			

INVENTEC

543016 60.3.31: ALL UNUSED GPIOs (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION



	MB_ID	MB_ID2	MB_ID3
	X01	0	0
	AX1	0	1
	AX2	1	0
	MP	1	1



INTEL_H23951_BGA_1356P

INVENTEC

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Block		Diagram	
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Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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GPU

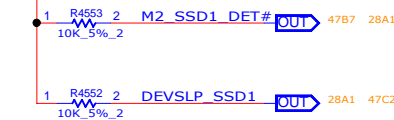
LAN

WLAN

HDD

SSD 4X

P3V3S

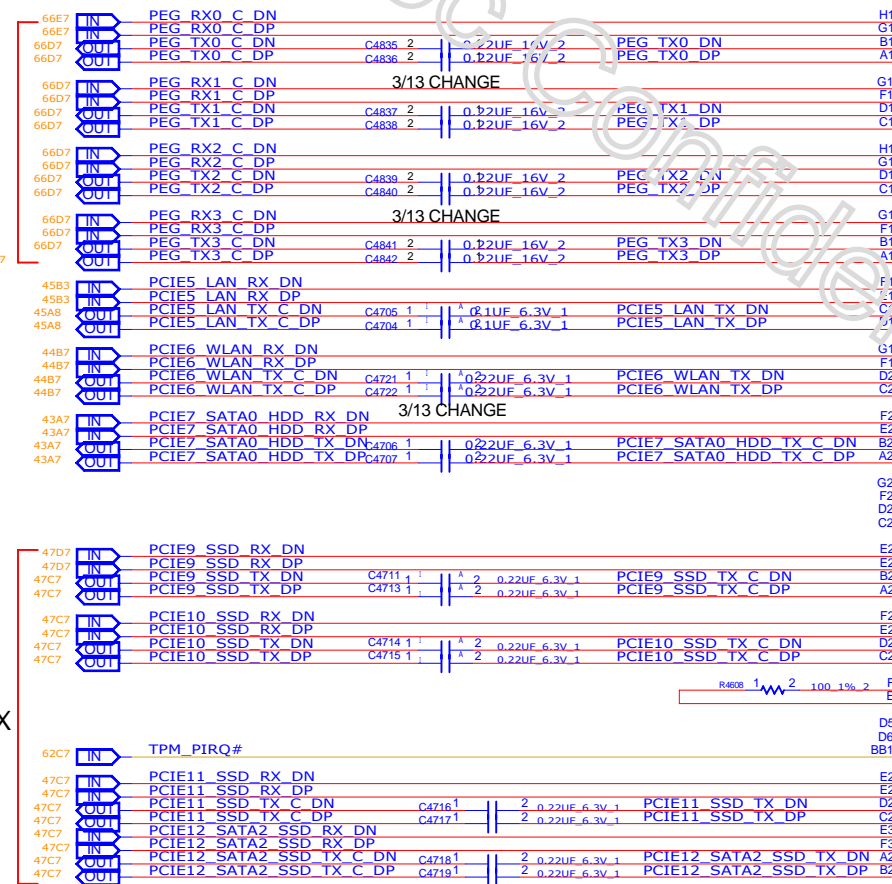
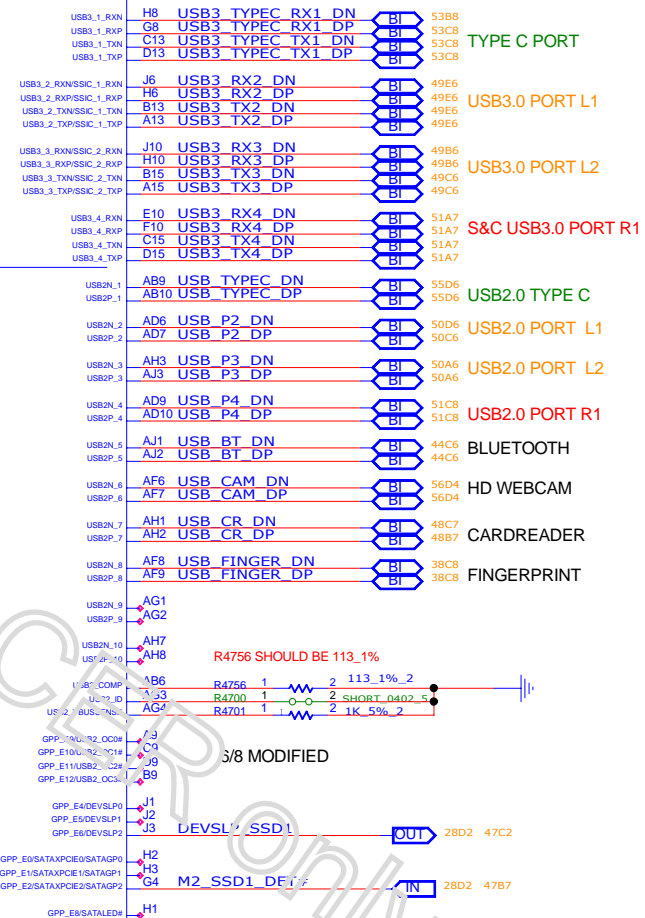


U4500

SKL_ULT

PCIE/USB3/SATA

SSIC / USB3



REFER PDG CHAPTER 36

DESIGN CONSTRAINT: FOR PCIE* GEN 3/ SATA MULTIPLEXED CONFIGURATION, MOTHERBOARD TX REQUIRES A 220NF CAPACITOR AND NO AC CAPACITOR IS REQUIRED FOR MOTHERBOARD RX CHANNEL

INTEL_H23951_BGA_1356P

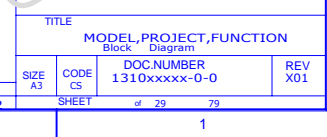
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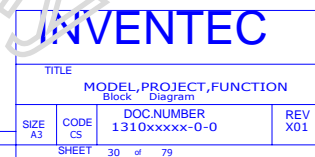
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MODEL PROJECT FUNCTION
Block Diagram

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PCB PIN 60xxxxxxxxx PCB VER XING>

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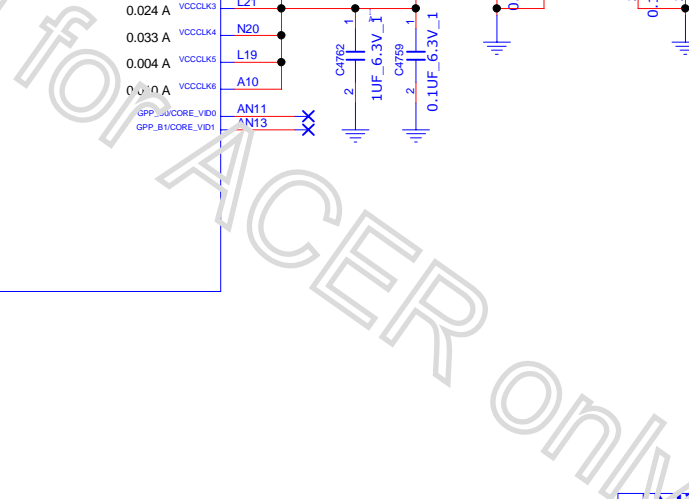






TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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4700-49,9(PCH)



TITLE	MODEL,PROJECT,FUNCTION
	Block Diagram

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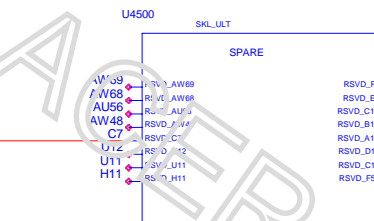
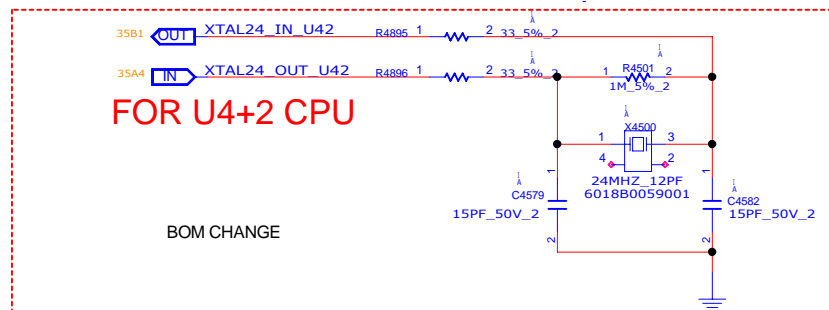
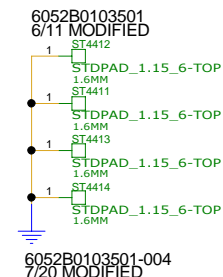
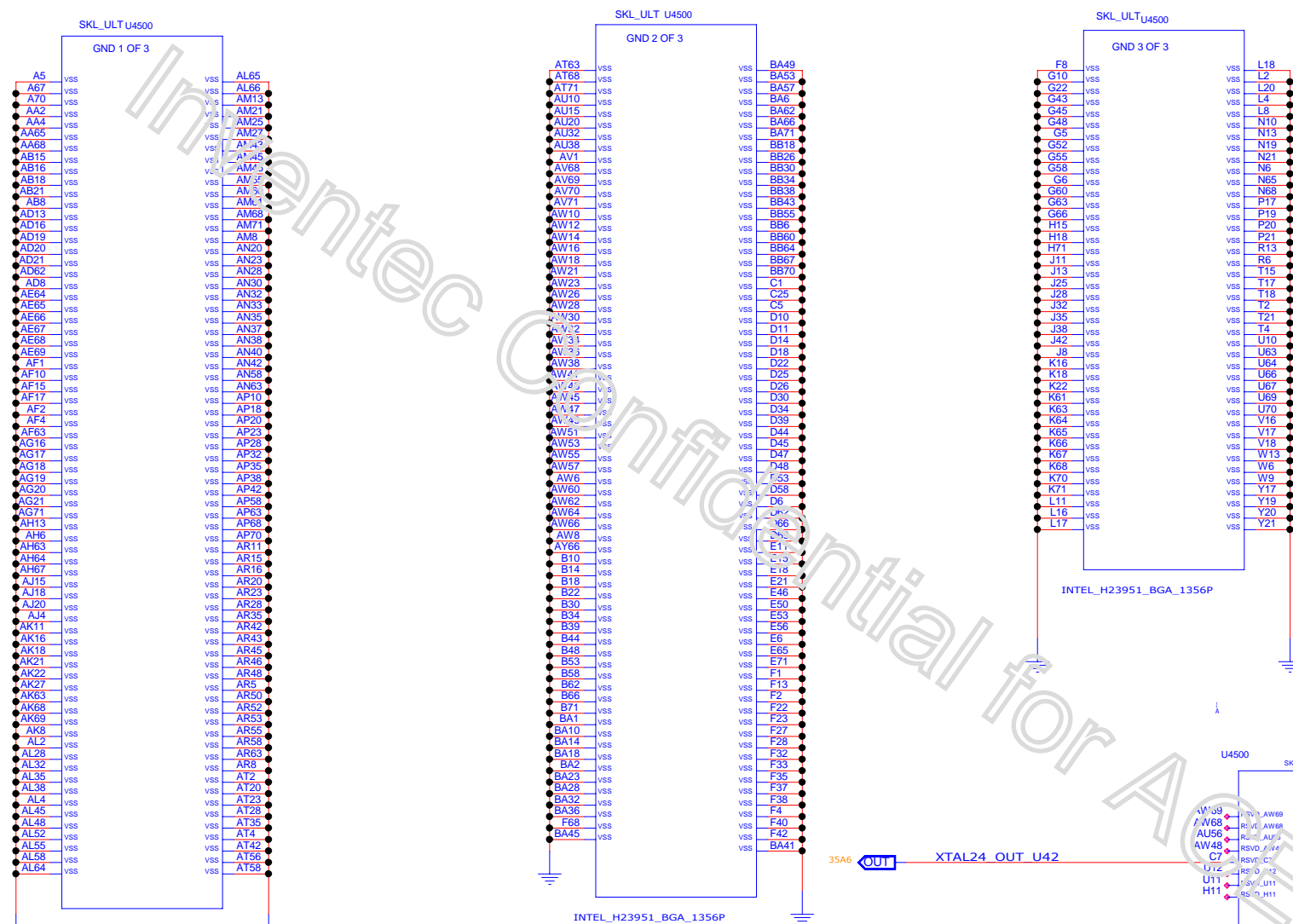
A

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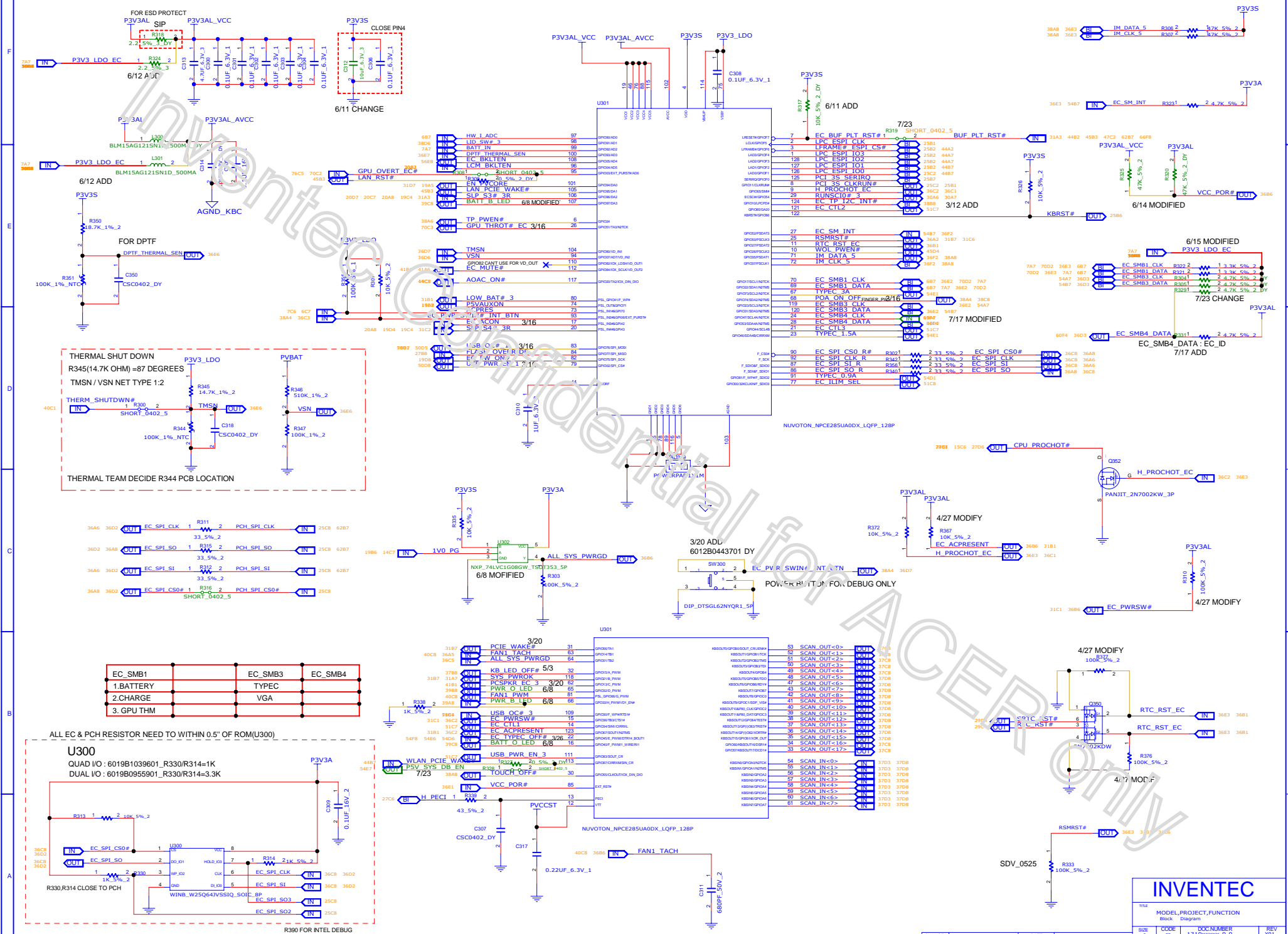
INTEL_H23951_BGA_1356P
For I²C Control Mode only(I2C_EN=H)
ADDR: I²C control bus address LSB. Internally pulled down at 150kΩ, 3.3V I/O.
[ADDR] =
L: 0x20/0x21
H: 0x22/0x23

INVENTECTITLE
MODEL,PROJECT,FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

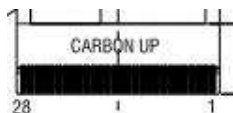
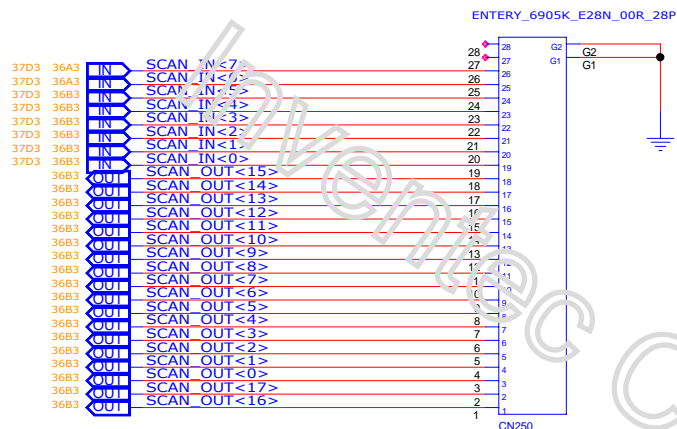
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PCB P/N 60xxxxxxx PCB VER XVER>

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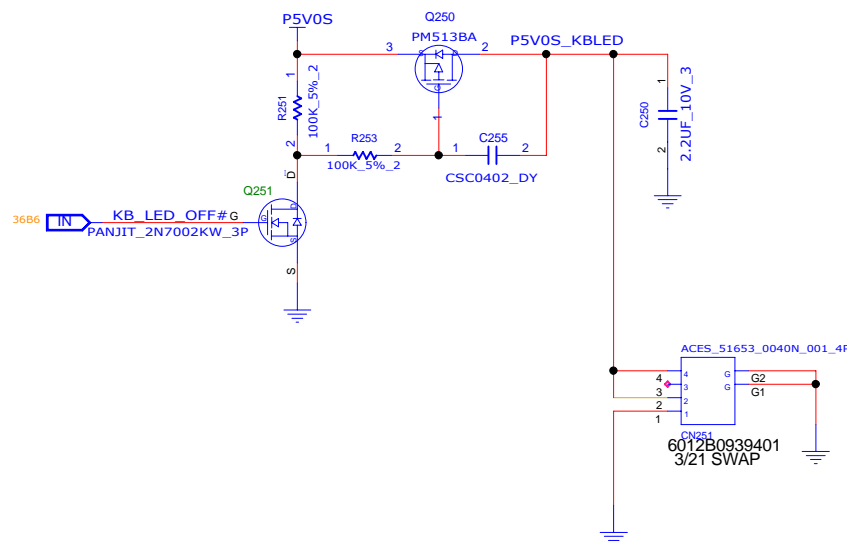
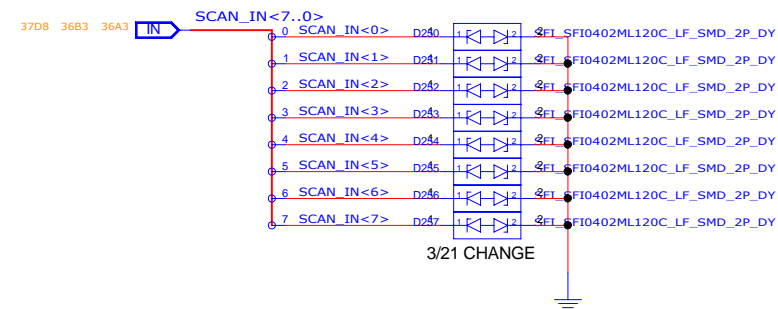


REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)

KEYBOARD CONN



	14*
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R10
28	R11



KEYBOARD LED CONN

VCC : +5V
LED Vf : 2.9~3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.9V)
Power consumption	228.71mA	320.2mA



INVENTEC

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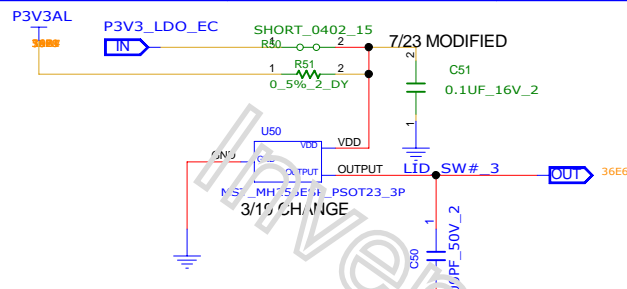
A

D

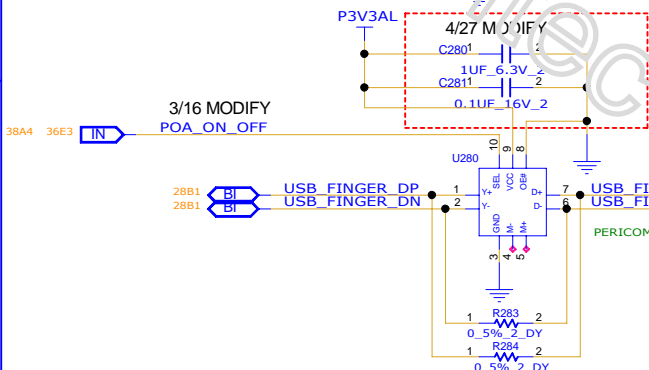
C

B

A



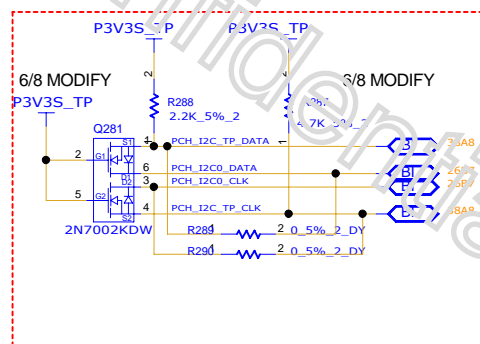
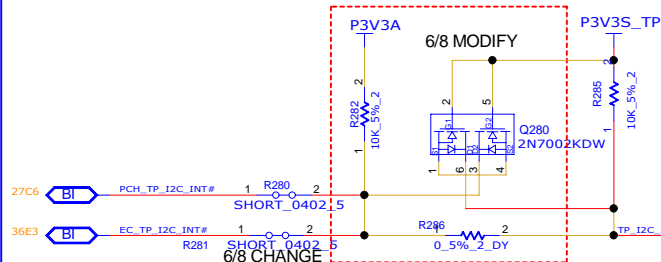
Signal Name	Active H/L	Direction	Description
POA_EN#	Low	Host to FPR	to activate the POA functionality
POA_POWERREQ	High	FPR to Host	To request additional power while acquiring/matching fingerprint
PWR_INT#	Low	FPR to Host	trigger power on event to EC
Auth_ERR	High	FPR to Host	to notify EC to error pattern LED or message
USB_SW_EN	High		Enable USB LS SW
FP_PWREN	High		control FP switch power enable



Truth Table

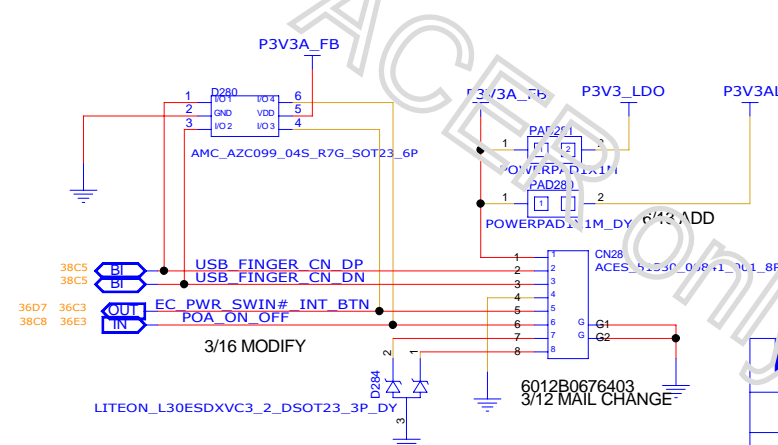
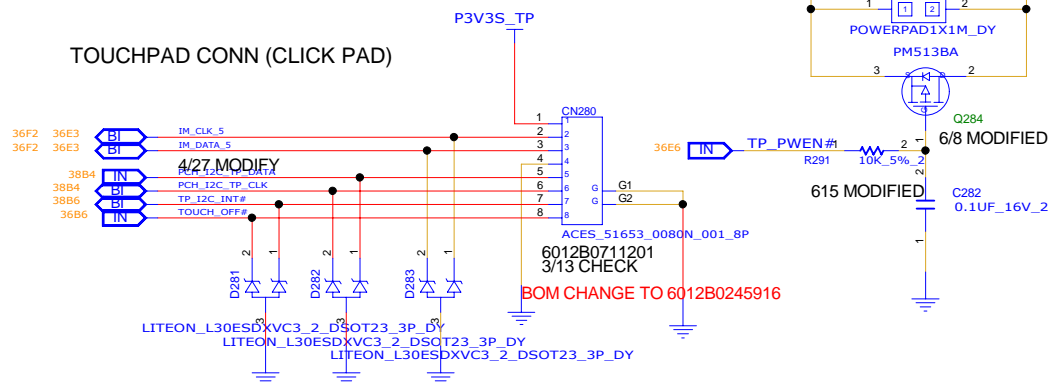
SEL	OE	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

Pin Number	Pin Definition
1	+FP_VCC
2	USBP
3	USBN
4	GND
5	POA_EN
6	PWR_INT#
7	AUTH_ERR
8	POA_POWERREQ



Pin	Name	IO	Active	Description
1	VCC	POWER		Power Supply for this module
2	D+	I/O		USB data+
3	D-	I/O		USB data-
4	GND	GND		Ground
5	INTN	O	Low	Button interrupt trigger; Short pulse in duration of 100 msec +/- 5%
6	Power_Ready	I		EC Power On/Off Notification; High: Power On, Low: Power Off
7	LED1	O		LED for R/G/B (optional)
8	LED2	O		LED for R/G/B (optional)

TOUCHPAD CONN (CLICK PAD)



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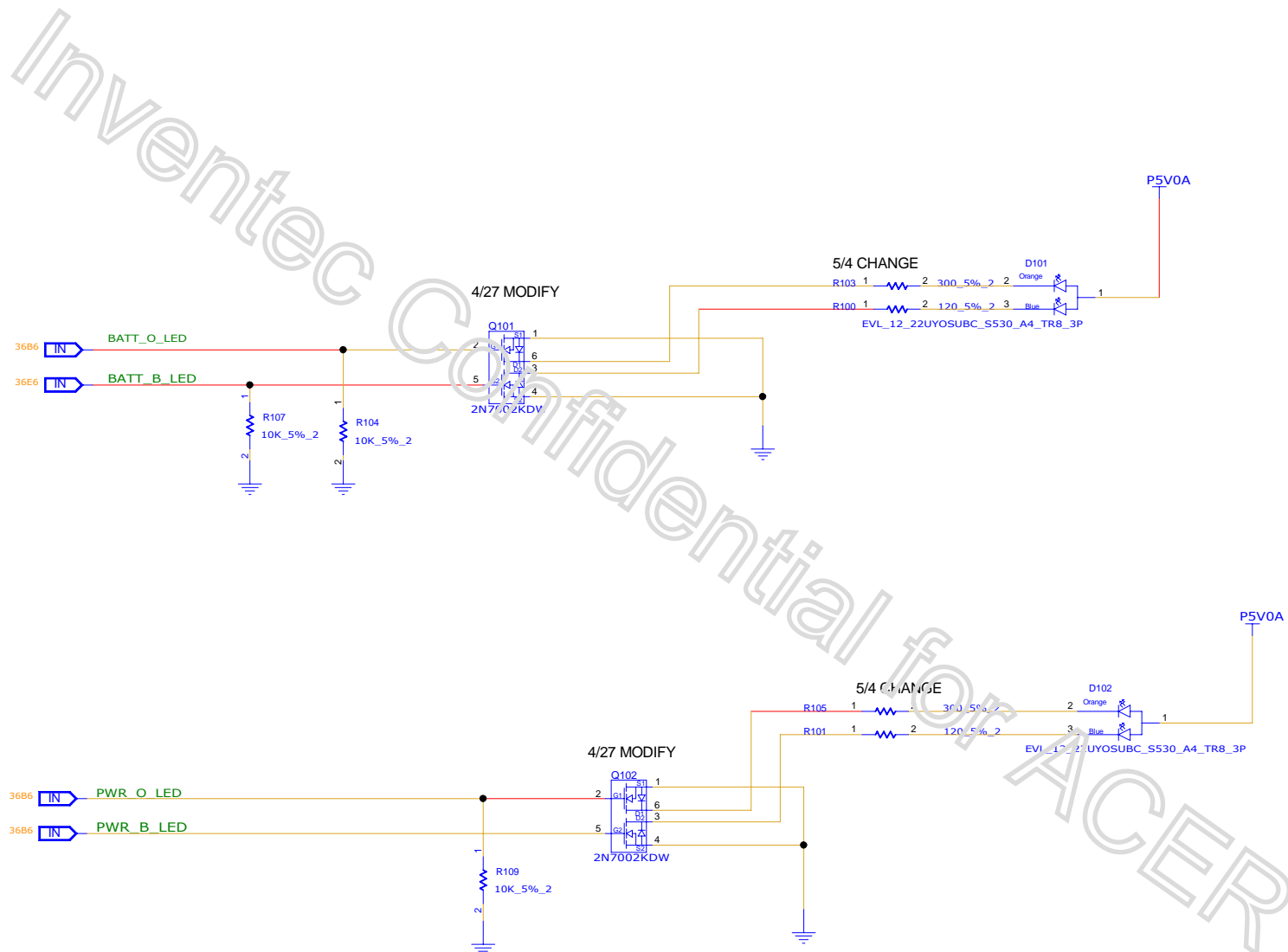
A

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A

**INVENTEC**TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE
PCB P/N 6PBGxxxxxxx PCB VER XXX-OCT-2002

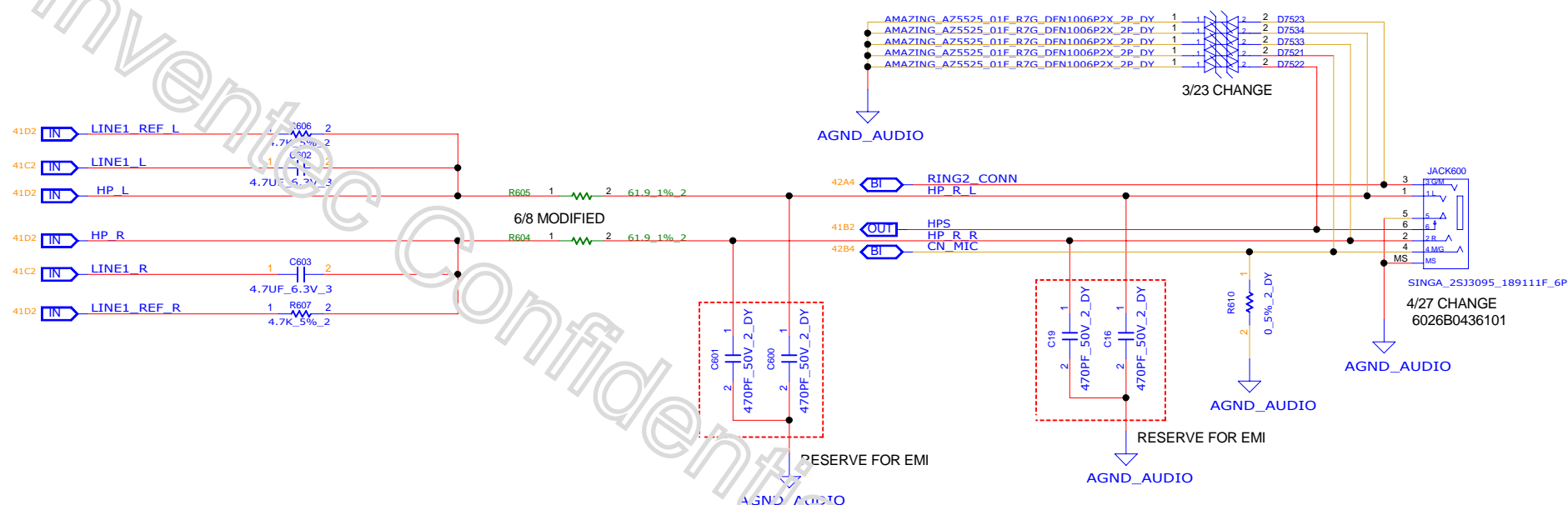
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PCB P/N	60NG-xxxxxxx	PCB VER	XXX-OCT-2002



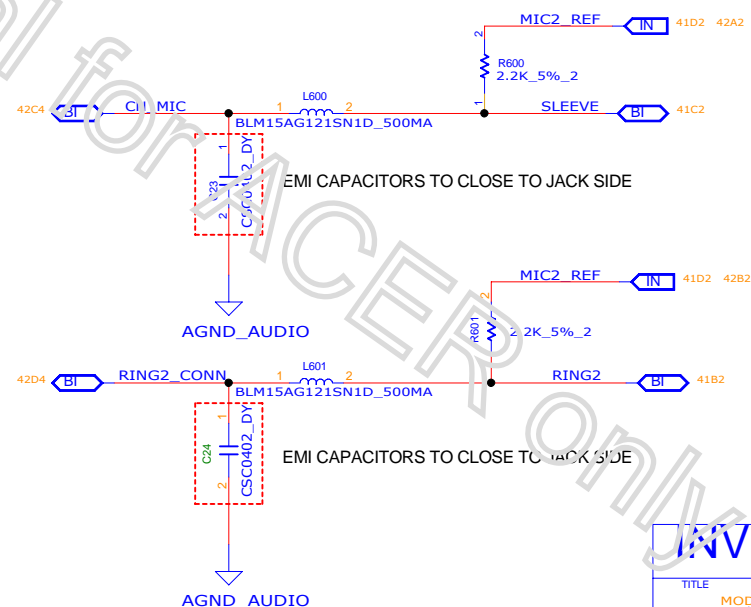
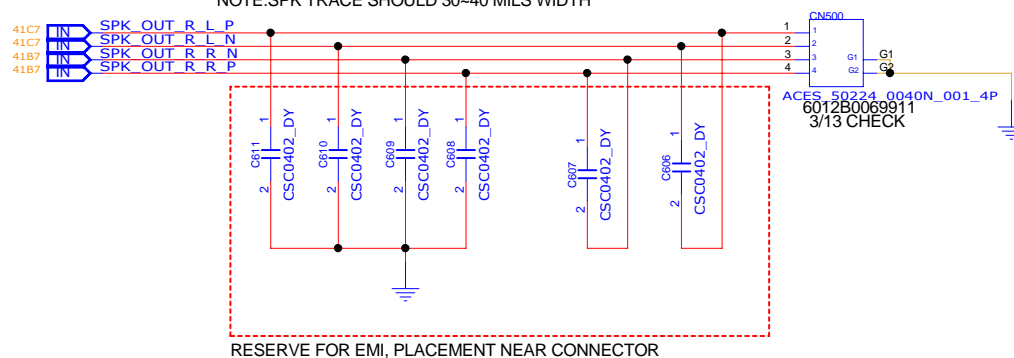
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MODEL,PROJECT,FUNCTION			
		Block	Diagram
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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AUDIO JACKS



INTERNAL SPEAKERS1

NOTE:SPK TRACE SHOULD 30~40 MILS WIDTH

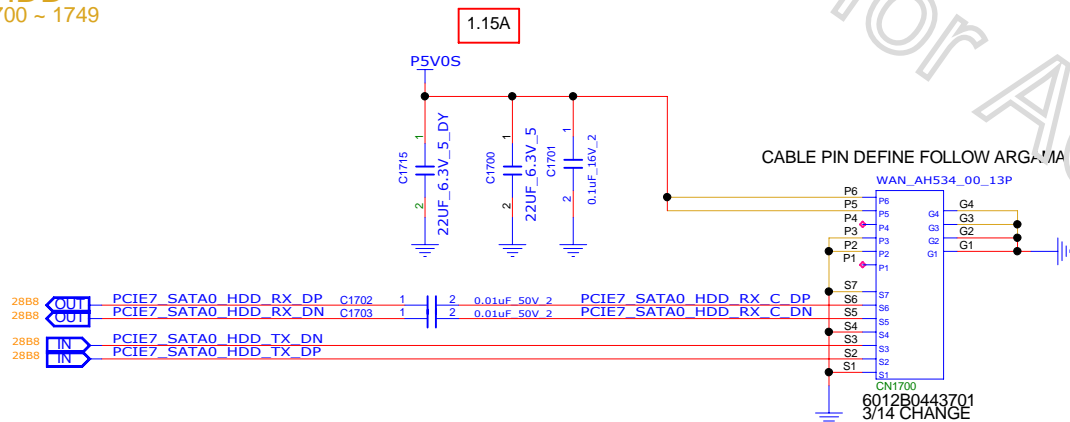


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MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		42 of 79	

CHANGE by	XXX	DATE	21-OCT-2002
PCR P/N	60xxxxxxxxxx	PCR VER	YYY

SATA HDD
Location 1700 ~ 1749

SATA HDD CABLE CONN on MB



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 43 of 79			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

A



SHEET 44 of 7

LAN (Controller)

Location 400 ~ 469

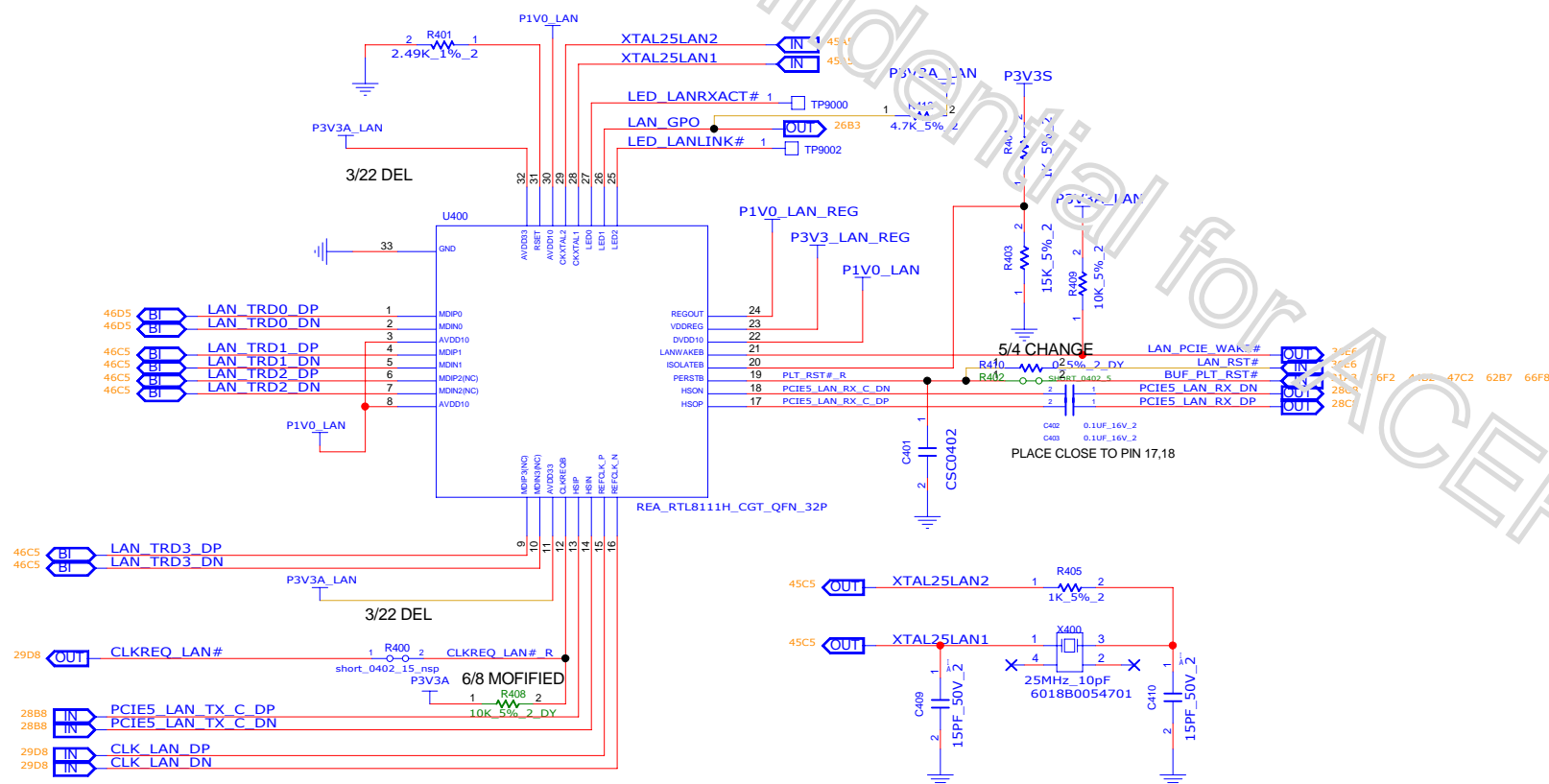
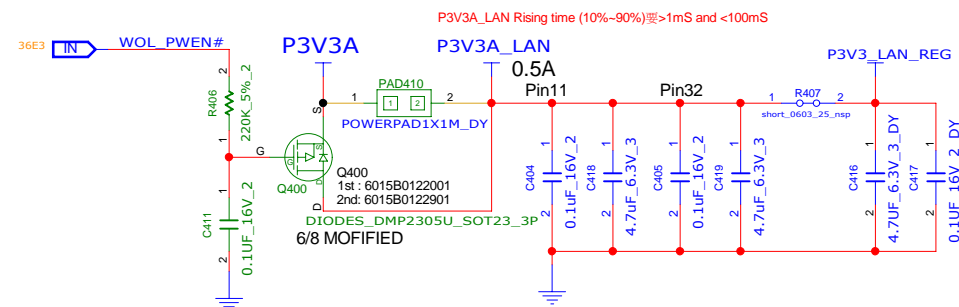
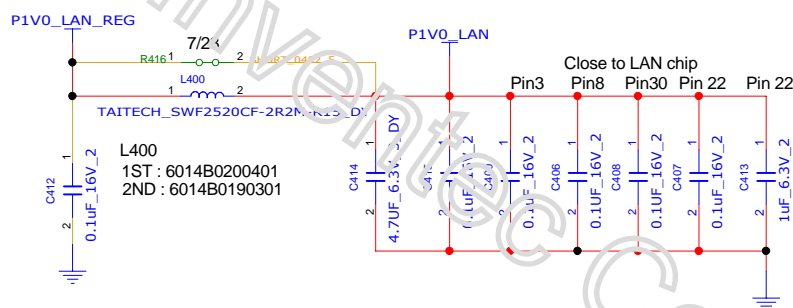
Ver.03_210120807

The schematic check had some item must modify as below.

01. 請註記 P3V3A_LAN Rising time (10%~90%)要>0.5mS and <100mS.

02. LAN power Noise P3V3A_LAN < 200mV Vpeak to Vpeak.

03. LAN power Noise P1_LAN < 100mV Vpeak to Vpeak.

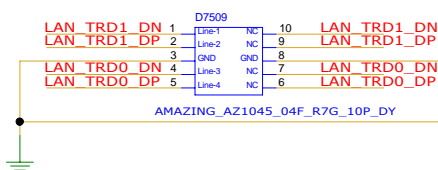
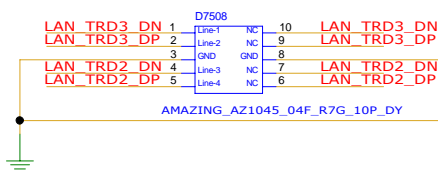
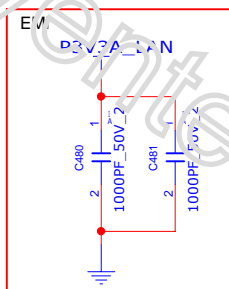


INVENTEC

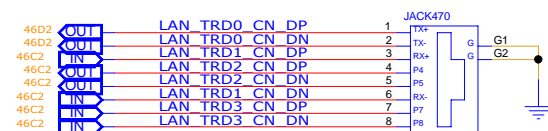
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MODEL,PROJECT,FUNCTION			
Block Diagram			
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A3	CS	1310xxxx-0-0	X01
SHEET 45 of 79			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

Location 470 ~ 499
Ver.01_20120801

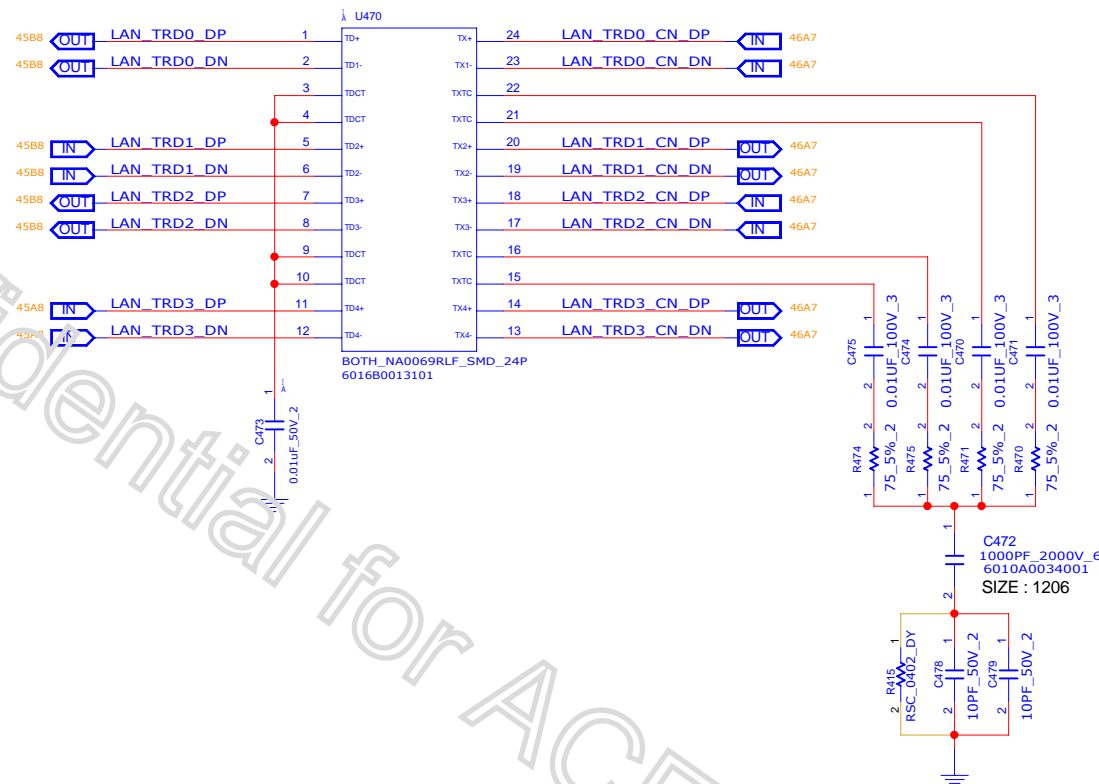


RJ-45



SINGA_2RJ1792_011111F_8P

4/27 MODIFY
6026B0435701

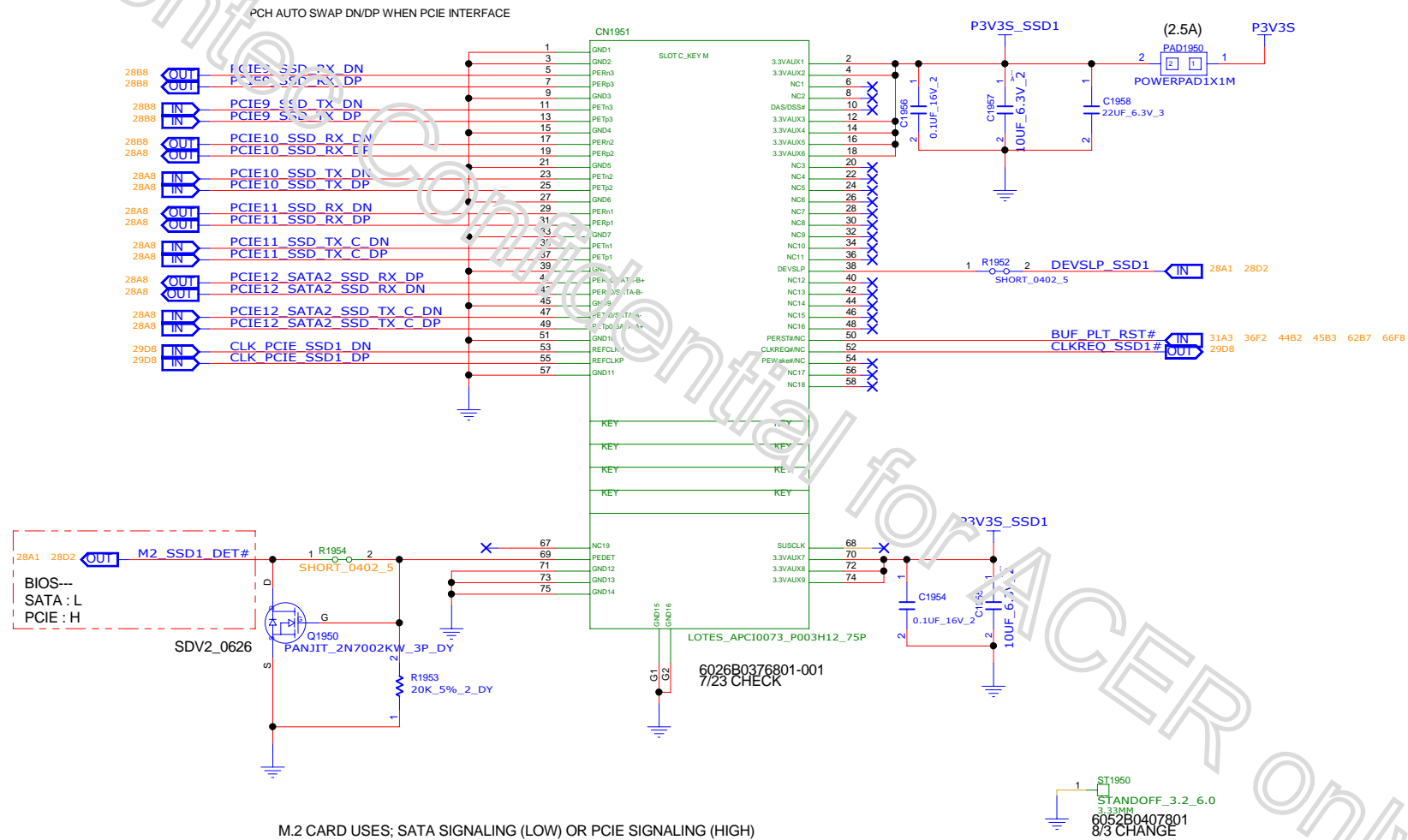


INVENTEC

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MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 46 of 79			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

NGFF SSD(PCIE/SATA 4X)



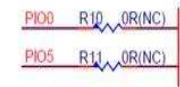
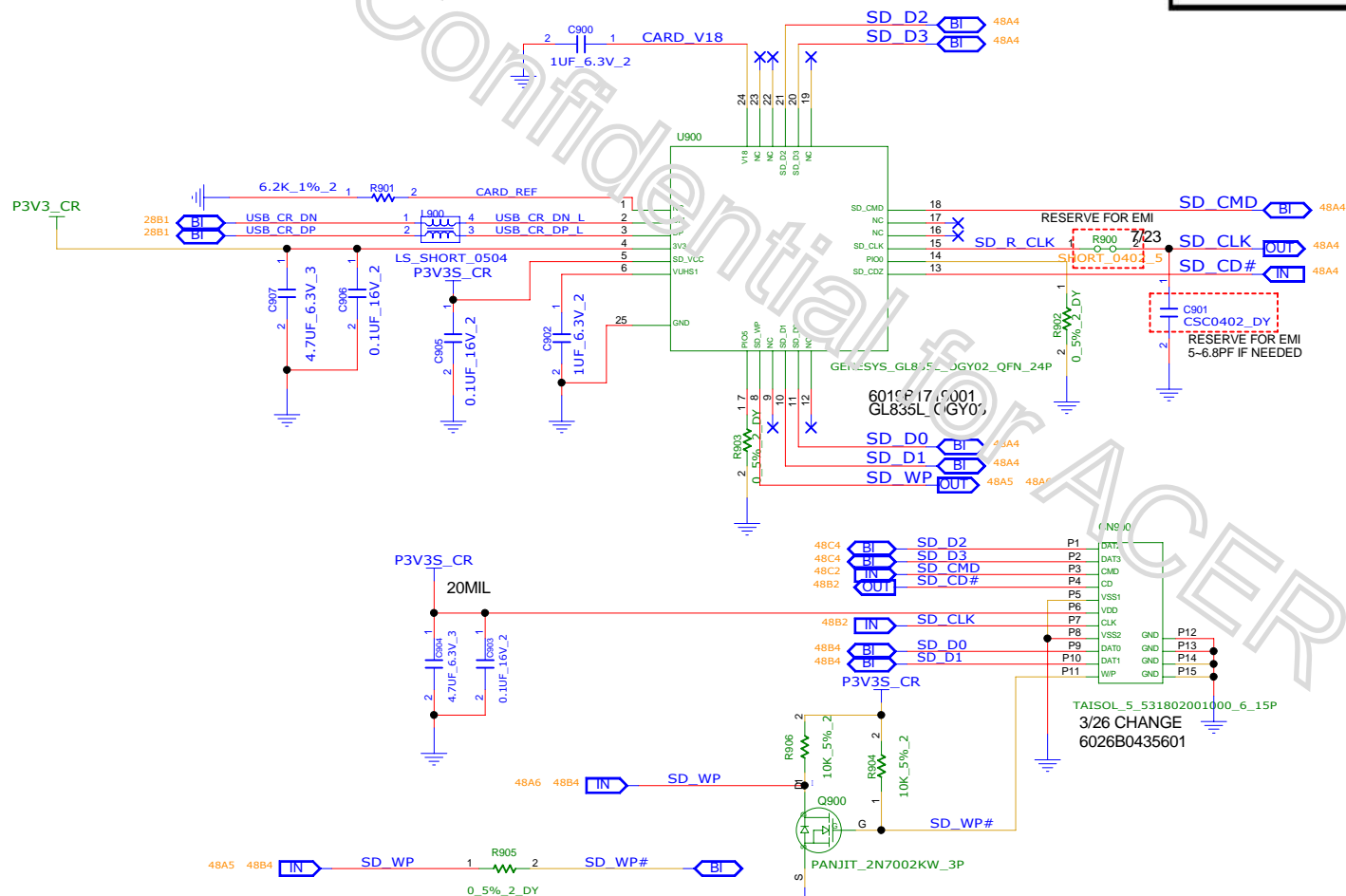
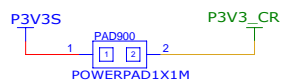
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

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TITLE MODEL,PROJECT,FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 47 of 79			

REFERENCE 900~999(CARDREADER)

CARD READER



	NC	OR
R10	Power Saving Mode	Disable Power Saving Mode
R11	No Support MMC Card	Support MMC Card

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
CARD READER

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxx PCB VER XXX

SHEET 48 of 79

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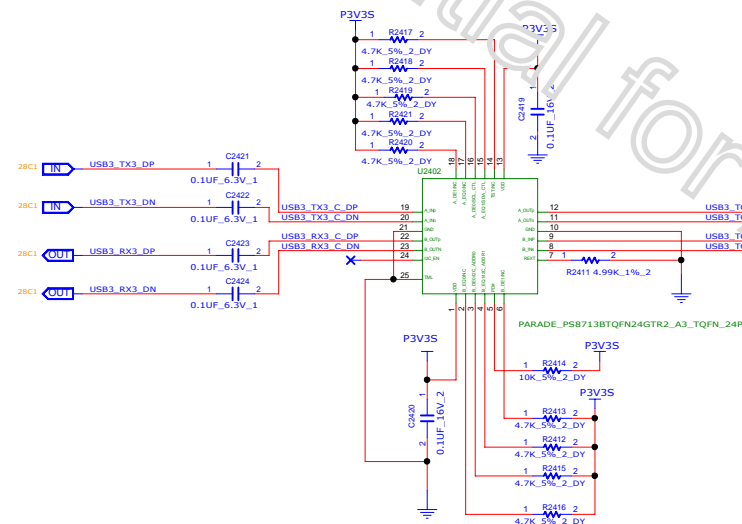
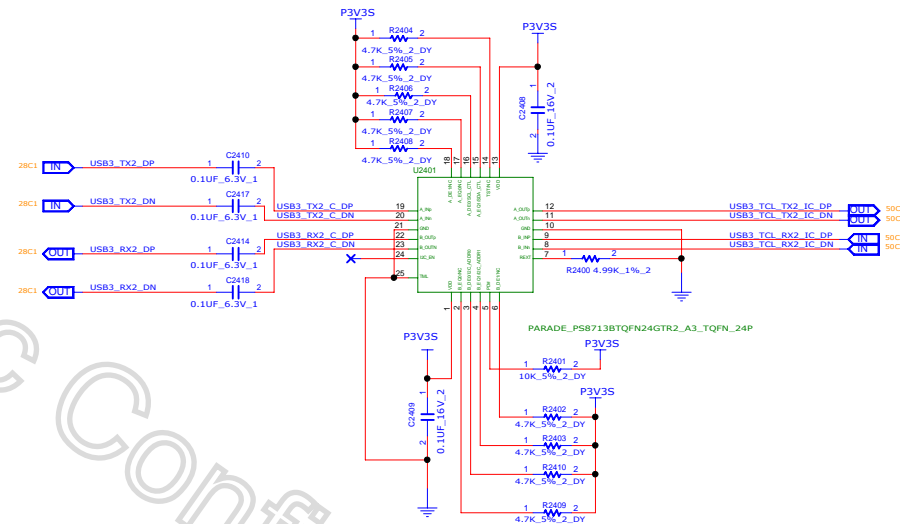
E

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**INVENTEC**TITLE
MODEL,PROJECT,FUNCTION

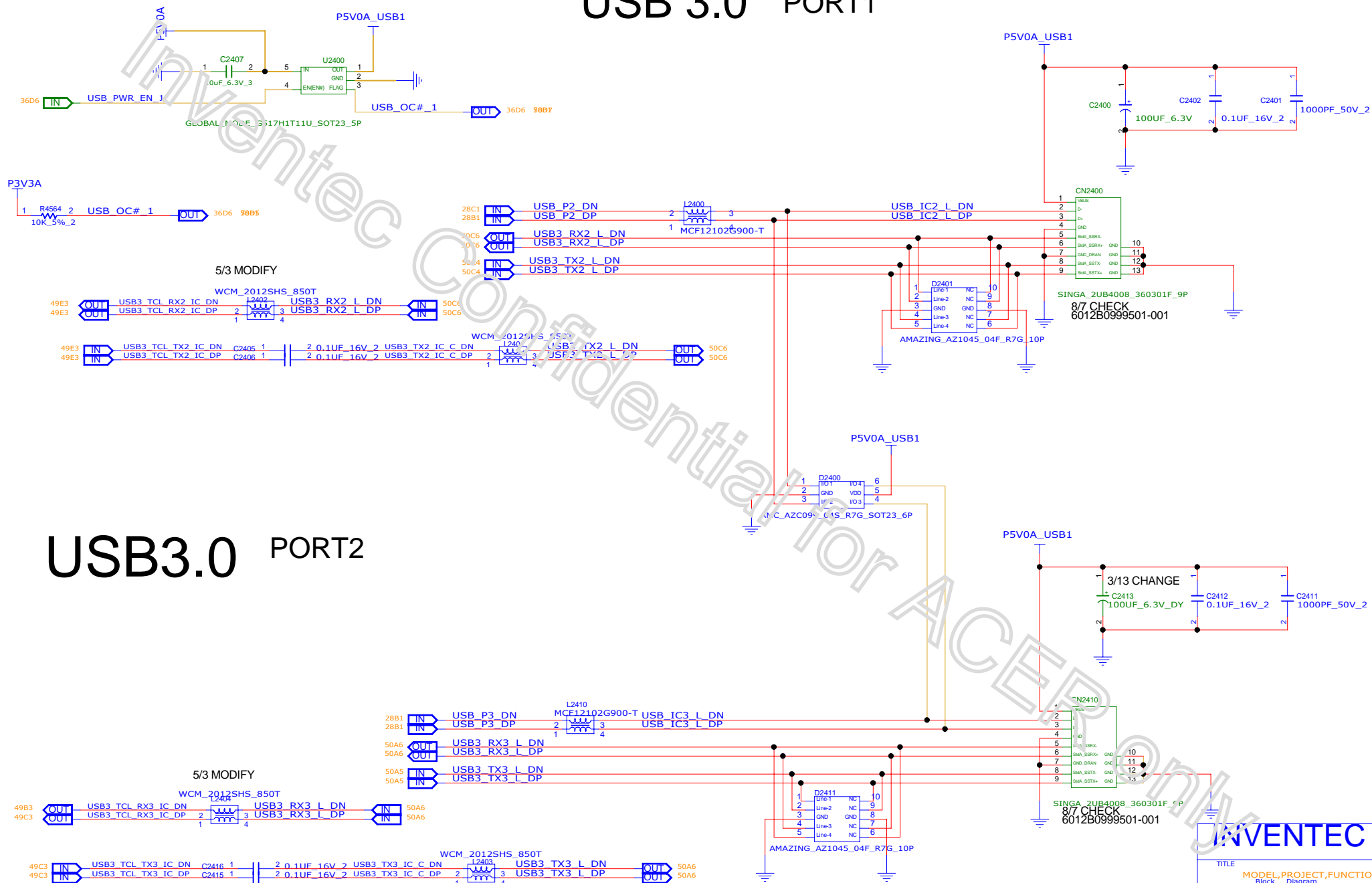
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C CS 1310xxxxx-0-0 X01

SHEET # 49 79

CHNGEN: XXXX DATE: 21-OCT-2002
PCB PIN: 60xxxxxx PCB VER: <REV>

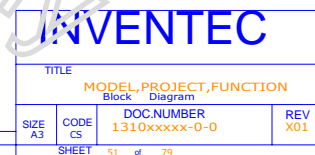
USB3.0 PORT2



INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	50	of	79		

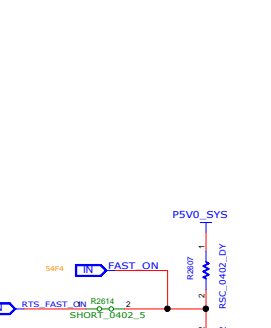
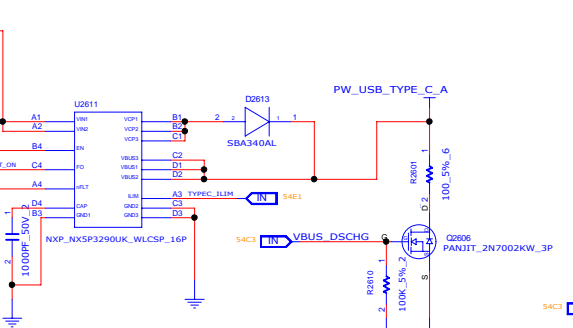
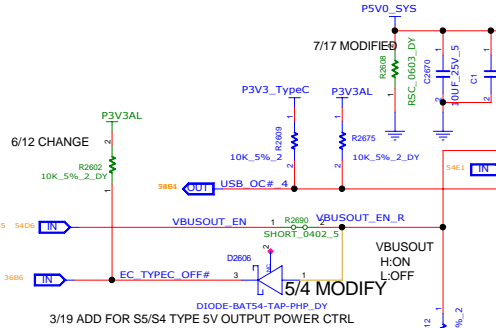
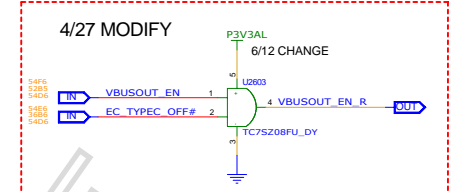
USB 3.0 PORT3





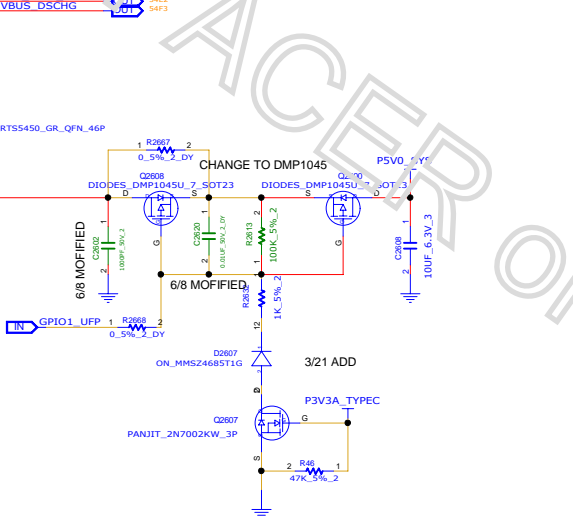
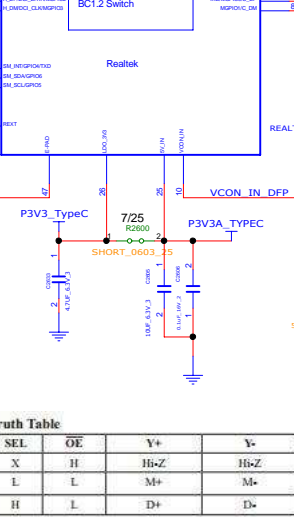
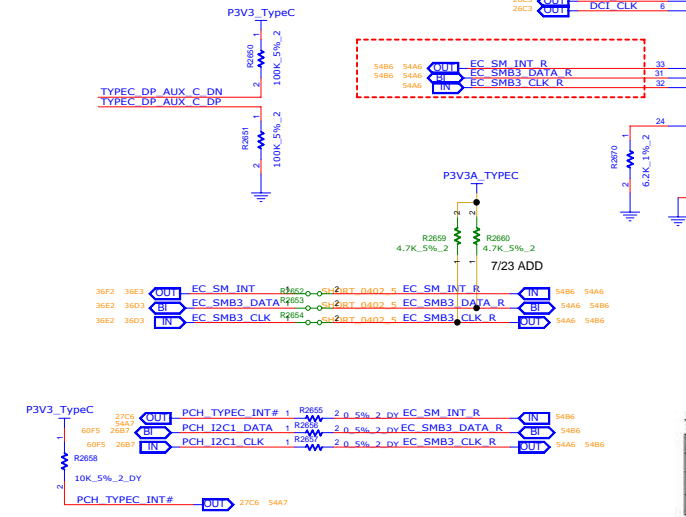
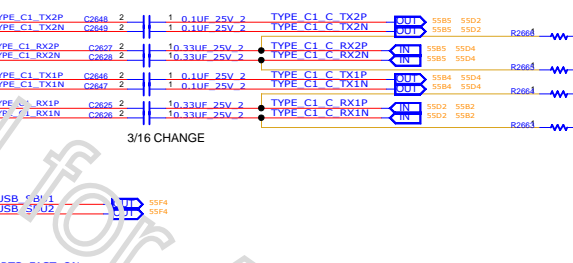
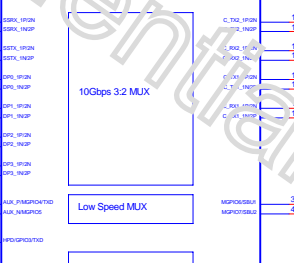
TITLE			
MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		52 of 79	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

53C2	OUT	USB3_TCL_RX_IC_DP	C2668	1	0.22UF 6.3V 1	USB3_TCL_RX_IC_C_DP	39	IN	USB3_TCL_RX_IC_C_DP	39
53C2	OUT	USB3_TCL_RX_IC_DN	C2668	2	0.22UF 6.3V 1	USB3_TCL_RX_IC_C_DN	40	IN	USB3_TCL_RX_IC_C_DN	40
53C3	OUT	USB3_TCL_TX_IC_DP	C2667	1	0.22UF 6.3V 1	USB3_TCL_TX_IC_C_DP	41	IN	USB3_TCL_TX_IC_C_DP	41
53C3	OUT	USB3_TCL_TX_IC_DN	C2667	2	0.22UF 6.3V 1	USB3_TCL_TX_IC_C_DN	42	IN	USB3_TCL_TX_IC_C_DN	42
57C2	IN	TYPEC_DP_TX0_DP	C2652	1	0.1UF 6.3V 1	TYPEC_DP_TX0_C2_DP	35	IN	TYPEC_DP_TX0_C2_DP	35
57C2	IN	TYPEC_DP_TX0_DN	C2652	2	0.1UF 6.3V 1	TYPEC_DP_TX0_C2_DN	36	IN	TYPEC_DP_TX0_C2_DN	36
57C2	IN	TYPEC_DP_TX1_DP	C2658	1	0.1UF 6.3V 1	TYPEC_DP_TX1_C2_DP	43	IN	TYPEC_DP_TX1_C2_DP	43
57C2	IN	TYPEC_DP_TX1_DN	C2658	2	0.1UF 6.3V 1	TYPEC_DP_TX1_C2_DN	44	IN	TYPEC_DP_TX1_C2_DN	44
57C2	IN	TYPEC_DP_TX2_DP	C2658	1	0.1UF 6.3V 1	TYPEC_DP_TX2_C2_DP	45	IN	TYPEC_DP_TX2_C2_DP	45
57C2	IN	TYPEC_DP_TX2_DN	C2658	2	0.1UF 6.3V 1	TYPEC_DP_TX2_C2_DN	46	IN	TYPEC_DP_TX2_C2_DN	46
57C2	IN	TYPEC_DP_TX3_DP	C2654	1	0.1UF 6.3V 1	TYPEC_DP_TX3_C2_DP	37	IN	TYPEC_DP_TX3_C2_DP	37
57C2	IN	TYPEC_DP_TX3_DN	C2654	2	0.1UF 6.3V 1	TYPEC_DP_TX3_C2_DN	38	IN	TYPEC_DP_TX3_C2_DN	38
57A1	IN	TYPEC_DP_AUX_DP	C2660	1	0.1UF 6.3V 1	TYPEC_DP_AUX_C_DP	1	IN	TYPEC_DP_AUX_C_DP	1
57A1	IN	TYPEC_DP_AUX_DN	C2660	2	0.1UF 6.3V 1	TYPEC_DP_AUX_C_DN	2	IN	TYPEC_DP_AUX_C_DN	2
57C1	IN	TYPEC_DP_HPDP	C2661	2	0.1UF 6.3V 1	TYPEC_DP_HPDP	34	IN	TYPEC_DP_HPDP	34

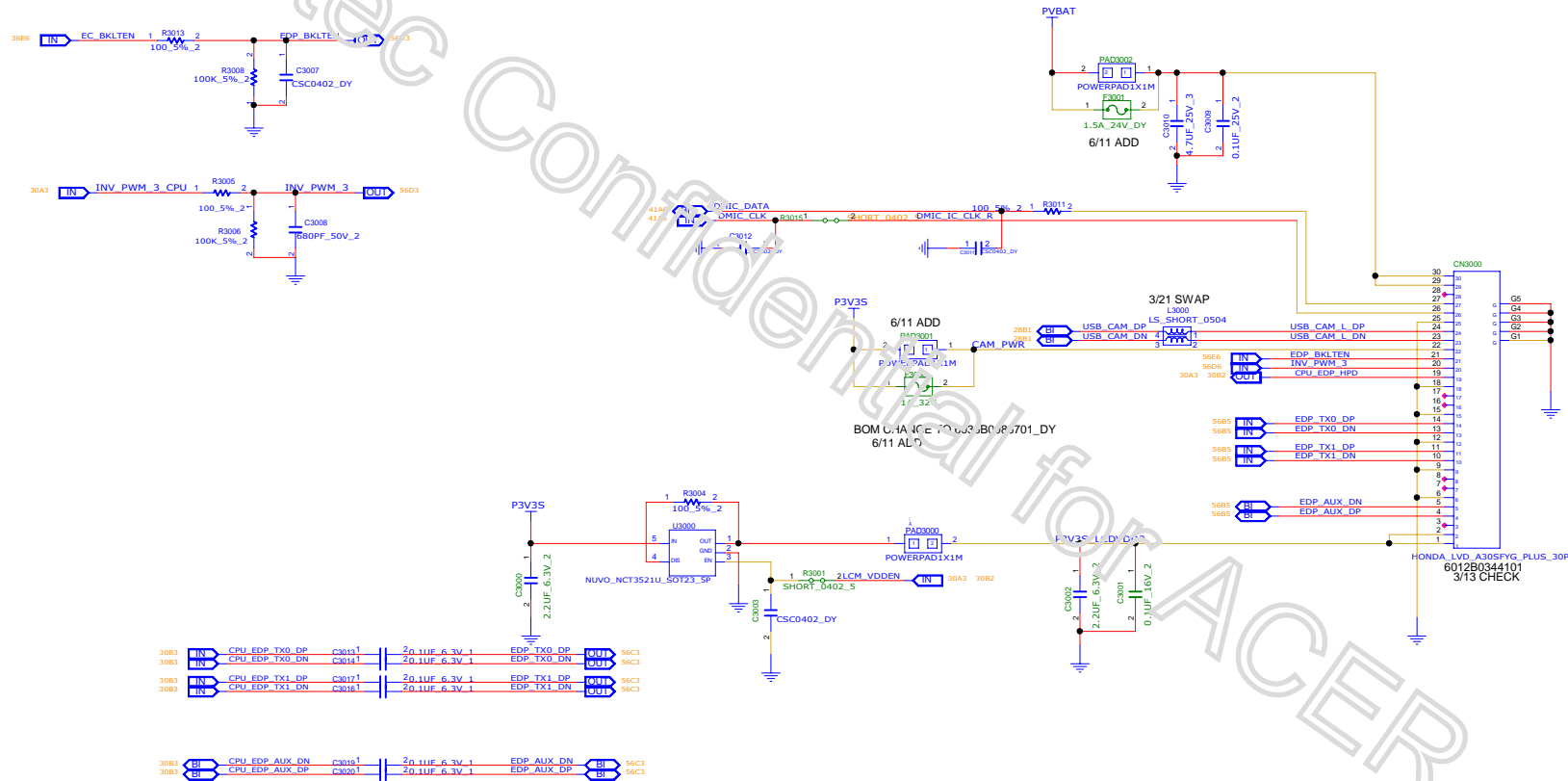




CHANGE b/	xxx	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	xvfr>

REFERENCE 3000~3049(LCM)

EDP CONN



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MODEL, PROJECT, FUNCTION			
Block	Diagram	Doc NUMBER	REV
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SHEET	50	4	70

CHANGES	DATE	21-OCT-2002
PCB PIN	PCB VER	XXXX

PS175



TITLE			
MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		58	of 79

CHANGE by	XXX	DATE	21-OCT-200
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

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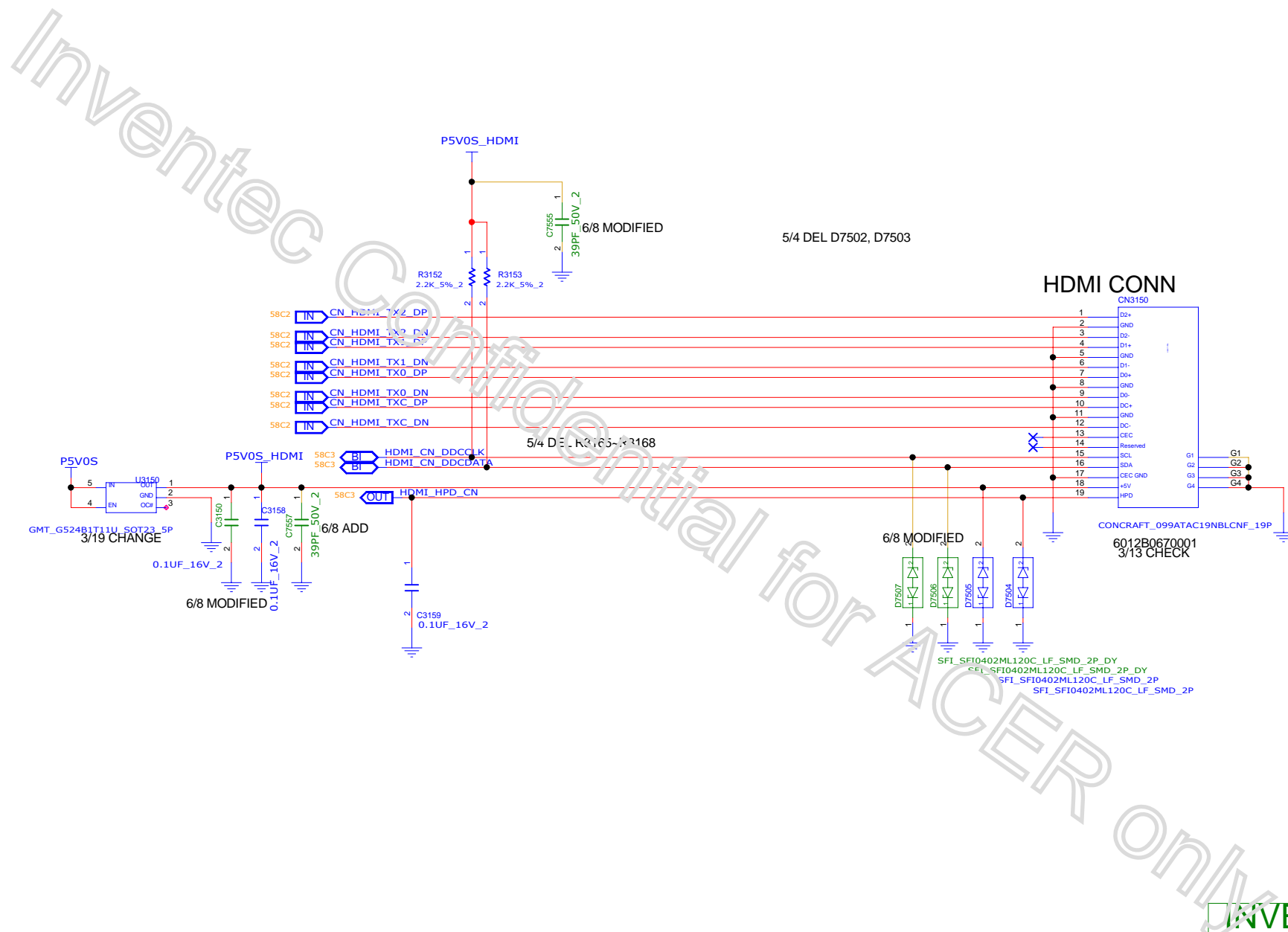
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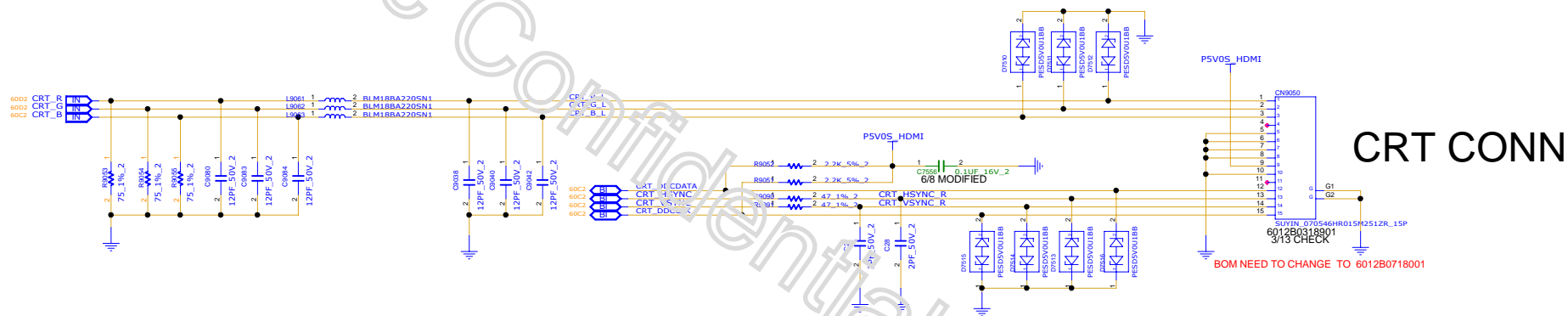
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INVENTEC

CHANGE by		DATE	TITLE	
PCB P/N		PCB VER	MODEL, PROJECT, FUNCTION	
XXX		21-OCT-2002	Block Diagram	
60xxxxxxxxxxx		XXX	DOC NUMBER	
			1310xxxxx-0-0	
			REV	
			X01	
			SHEET	
			59 of 79	



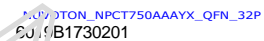


REFERENCE NUMBER:9050~9099

INVENTEC

Title			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310XXXXX-0-0	X01
SHEET	61	of 75	

CHGNGEN	XXX	DATE	21-OCT-2002
PCB PIN	60XXXXXXXXXX	PCB VER	XXX



SHEET 62 of 79

CHANGE by	XXX
PCB P/N	60xxxxxxxxxxx

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE SHEET	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		63	of 79

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INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
TP55450			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310XXXXX-0-0	X01
SHEET		#	64 79

CHGNGN	XXX	DATE	21-OCT-2002
PB PIN	60XXXXXXXXXX	PB VER	<WES>

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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

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MX130

GD5R5 23X23

6019B1722001 N16S-GTR-S-A2
6019B1720401 MT51J256M32HF-70 (MICRON)
6019B1720501 H5GC8H24AJR-R0C (HYUNIX) 2018.03.20

21-OCT-2002		
DATE	CHANGE NO.	REV
		A

Chan, Shene Huang, Vero			Shiu, Vivi			INVENTEC			
DESIGN/DRAWER			DATE			MODEL, PROJECT, FUNCTION			
CHECK			21-OCT-2002						
APPROVAL			A01			SIZE	CODE	DOC NUMBER	REV
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PCB PIN			PCB VER			SHEET			
S00000000000000000000			XXX			of 85 79			

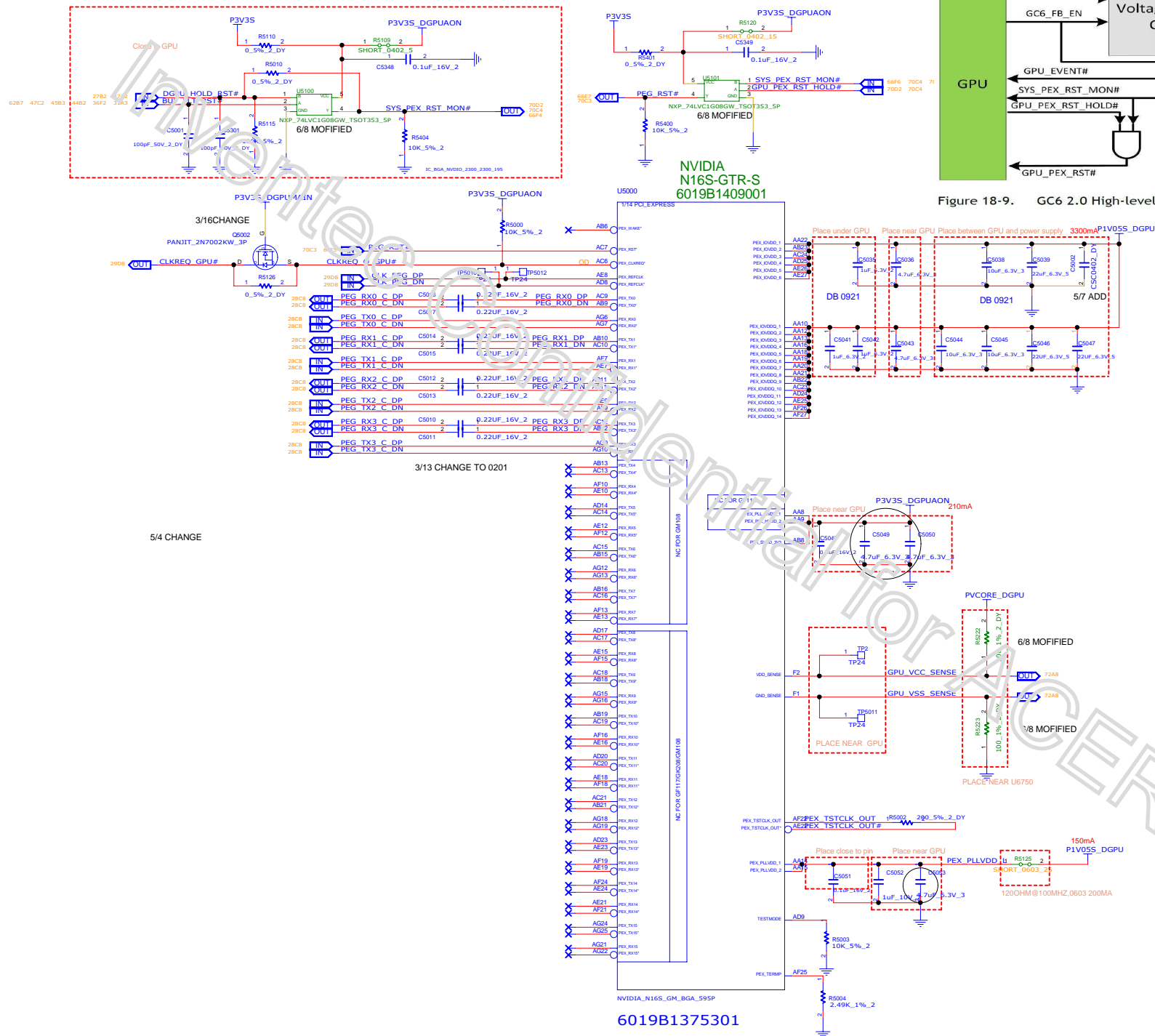
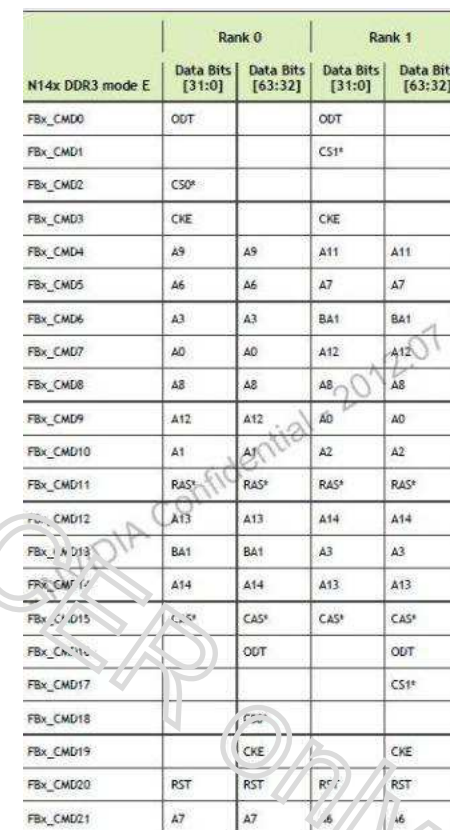


Figure 18-9. GC 2.0 High-level Signal Connection Concept

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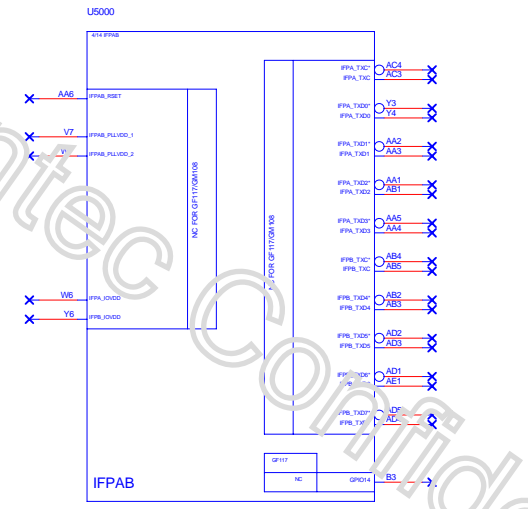
TITLE			
MODEL,PROJECT,FUNCTION			
GPU-1			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310XXXXX-0-0	X01
SHEET		#	66 79



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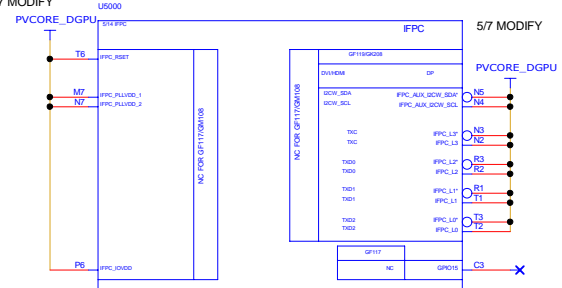
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NVIDIA_N16S_GM_BGA_595P

6019B1375301

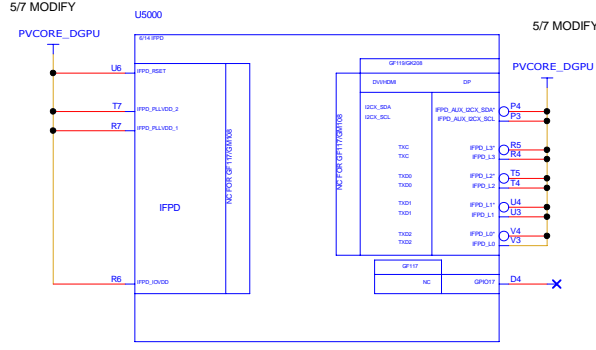
5/7 MODIFY



NVIDIA_N16S_GM_BGA_595P

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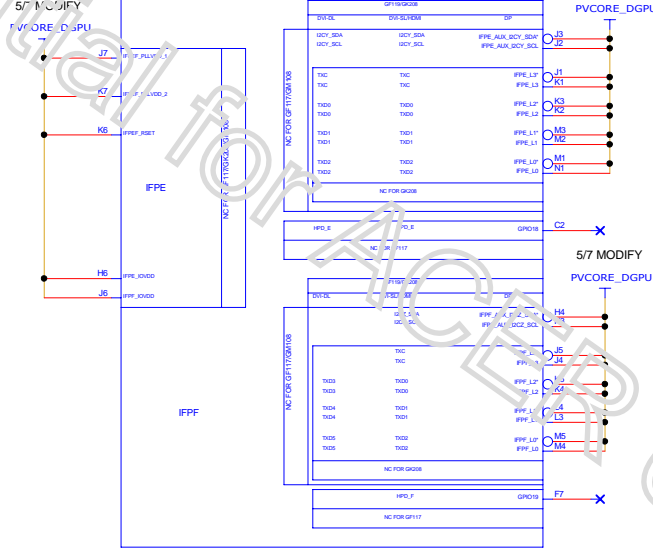
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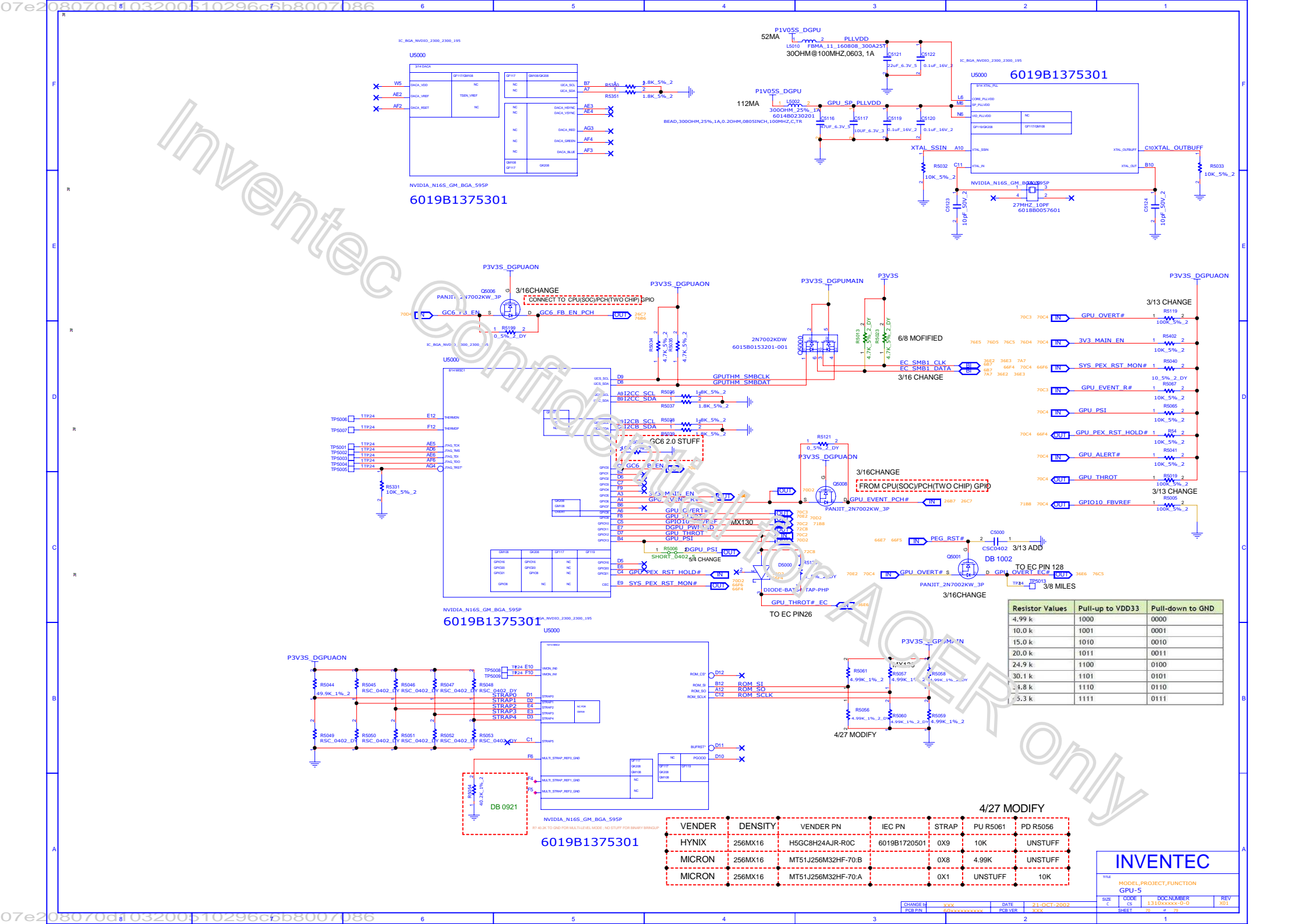
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INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION				
GPU-4				
SIZE	CODE	DOC NUMBER		REV
C	CS	1310xxxxxx-0-0		X01
SHEET 69 of 79				



VENDER	DENSITY	VENDER PN	IEC PN	STRAP	PU R5061	PD R5066
HYNIX	256MX16	H5GC8H24AJR-R0C	6019B1720501	0X9	10K	UNSTUFF
MICRON	256MX16	MT51J256M32HF-70:B		0X8	4.99K	UNSTUFF
MICRON	256MX16	MT51J256M32HF-70:A		0X1	UNSTUFF	10K

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MODEL,PROJECT,FUNCTION
GPU-5

SIZE
C

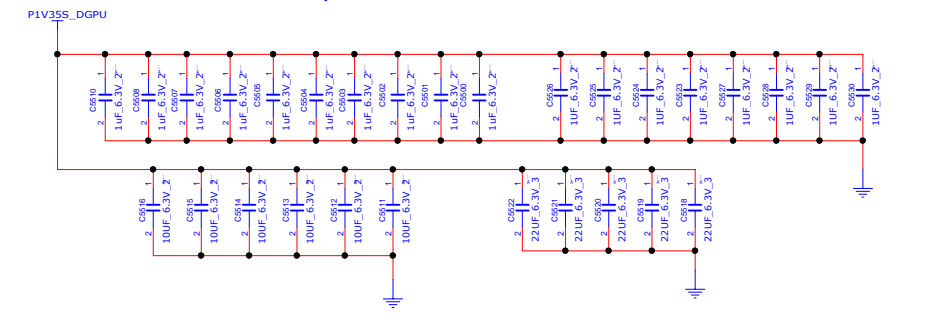
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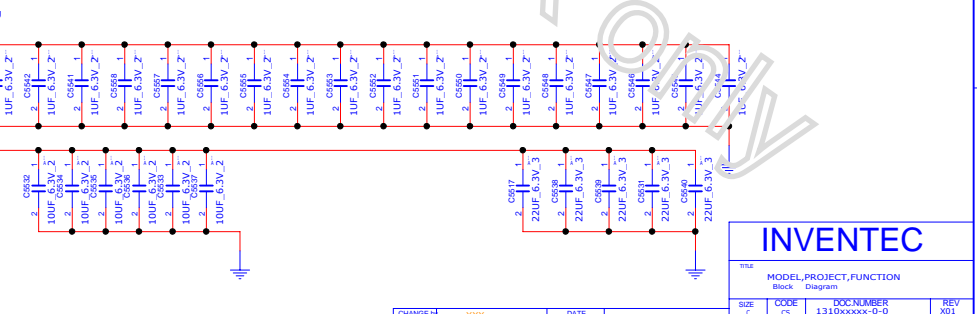
REV
001

CHANGES	XXXX	DATE	21-OCT-2002
PCB PIN	XXXXXXX	PCB VER	XXXX


M3=U5500
NON MIRROR



M4=U5501
MIRROR



INVENTEC

								<table><tr><td colspan="4">TITLE</td></tr><tr><td colspan="4">MODEL,PROJECT,FUNCTION Block Diagram</td></tr><tr><td>SHEET</td><td>CS</td><td>DOC NUMBER</td><td>REV</td></tr><tr><td></td><td></td><td>1310XXXXXX-0-0</td><td>X01</td></tr></table>				TITLE				MODEL,PROJECT,FUNCTION Block Diagram				SHEET	CS	DOC NUMBER	REV			1310XXXXXX-0-0	X01
TITLE																											
MODEL,PROJECT,FUNCTION Block Diagram																											
SHEET	CS	DOC NUMBER	REV																								
		1310XXXXXX-0-0	X01																								
CHANGE D	XXX	DATE		PCB PIN	6DENSEXXXX	PCB VER 2	QCT2002																				



22 1 A R67000 2 PVCORE_DGPU_SENSE OUT 72A5

The schematic shows a power pad connection. A signal line labeled E_DGPU2 is connected to the input of a component labeled PADS67011. The component has a '2' in a box and an 'A' next to it, indicating a 2A current source. The output of the component is connected to a line labeled PVBAT. The component is also labeled POWERPAD_2_0610.

50% CHANGE

5/8 CHANGE

5V

470uF 2V (C6, 02)

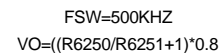
22uF 3V (C6, 04)

5.0V

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxxx-0-0	REV X01
SHEET 72 of 79			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



TITLE	MODEL, PROJECT, FUNCTION
Block	Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



SHEET 74 of 79

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

TITLE	MODEL,PROJECT,FUNCTION
	Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		75 of 79	

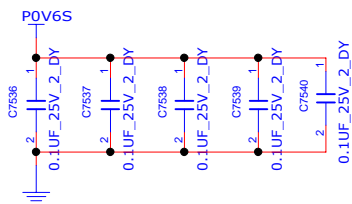
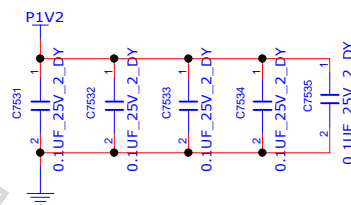
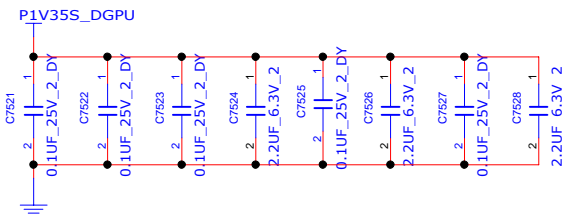
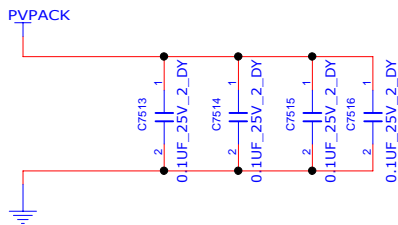
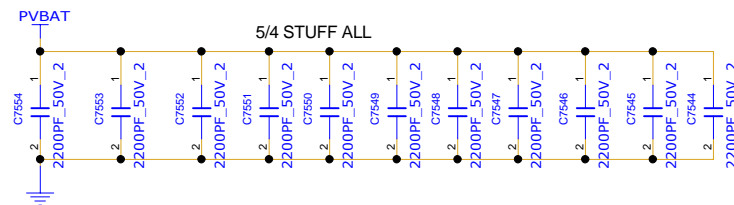
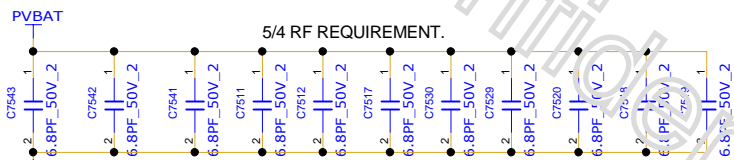
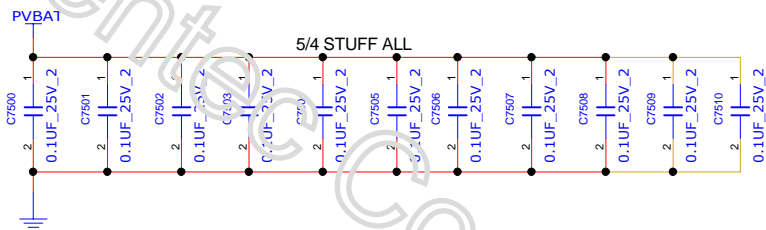


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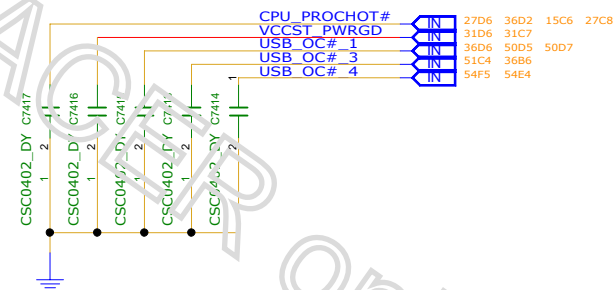
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MODEL,PROJECT,FUNCTION			
		Block	Diagram
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		77	of 79

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TITLE	MODEL,PROJECT,FUNCTION
	Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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